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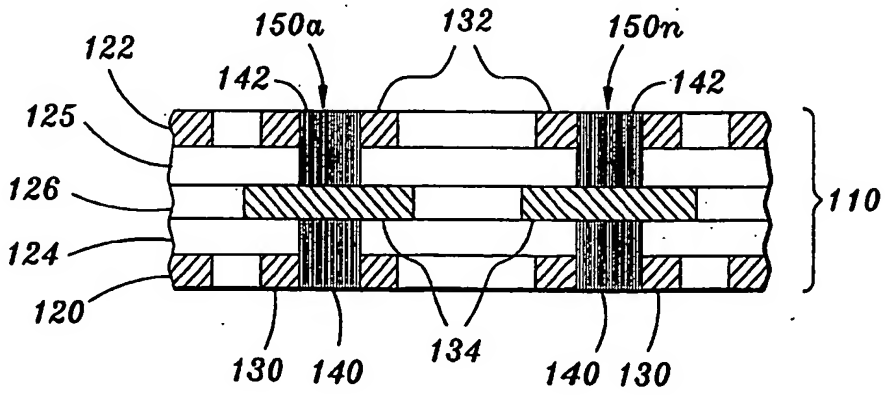
(54) Title: TELESCOPING BLIND VIA IN THREE-LAYER CORE



(57) Abstract: A multilayer PCB including at least one carrier, wherein the at least one carrier comprises a pseudo three-layer core (110). Each three-layer core (110) includes a first metal layer (120), a first dielectric layer (124), an internal bridge layer (126), a second dielectric layer (125), and a second metal layer (122). The bridge layer includes a plurality of bridge pads (134). Each carrier includes a plurality of interlayer interconnection units (150a, 150n) for interconnecting the first and second metal layers. Each interlayer interconnection unit comprises a pair of opposed blind vias (140, 142) and a bridge pad (134) disposed between, and in electrical contact with, the pair of blind vias.

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TELESCOPING BLIND VIA IN THREE-LAYER CORE

BACKGROUND OF THE INVENTION

[0001] The present invention generally relates to printed circuit boards, and more particularly to multilayer printed circuit boards comprising a three-layer core having a dual blind via interlayer interconnection unit. The present invention also relates to methods for forming a three-layer core of a multilayer printed circuit board.

[0002] The present trend in the design and manufacture of printed circuit boards (PCBs) is towards decreased size, smaller hole or via diameter, and higher interconnection density. High interconnection densities require multilayer PCBs having more than one signal layer with numerous interconnections therebetween.

[0003] Each signal layer of prior art multilayer PCBs typically consists of a patterned conductive metal layer. Adjacent conductive layers are separated by an insulating material or dielectric layer comprising, for example, a polyimide or a resin which may be reinforced with glass fiber. Interconnections between the various conductive layers are provided by holes or vias that extend through the intervening dielectric layer, wherein the vias or holes are plated, filled, and/or plated over with conductive material. Such vias or holes may be through holes, blind vias, or buried vias. Through holes extend to all conductive layers of a multilayer assembly. In contrast, blind vias and buried vias pass through only part of a PCB – blind vias having one end of the via exposed, and buried vias having neither end of the via exposed. Thus, a blind via connects two or more layers of a PCB and starts on an outer layer, but does not pass completely through the PCB. A buried via connects two or more inner layers of a PCB but no outer layer.

[0004] Two-layer cores, which consist of a thin dielectric layer covered with copper foil, form the basic building block of prior art PCBs. Typically, the dielectric layer of a two-layer core is covered with copper foil on both sides. Multilayer PCBs of the prior art may be formed by laminating two or more two-layer cores. After patterning the copper foil of the signal layers, the layers are laminated using heat and pressure. Plated via holes for interlayer connection may be formed by drilling in the z-axis between layers, e.g., by laser drilling, followed by plating the hole. A blind via may be formed by drilling partly through one or more dielectric layers, followed by

plating the hole, or by forming a plated through hole and then laminating an additional layer on one side thereof. A buried via may be formed by forming a blind via and laminating an additional layer on the exposed end of the blind via, or by providing a plated through hole and laminating an additional layer on each side of the plated through hole. Such procedures or processes are well known in the art.

[0005] As noted above, the standard building block of prior art PCBs is a core consisting of a two-layer dielectric carrier. Stacking a μvia on either side of such a carrier requires a solid target pad for laser ablating down to (or building up from with additive technology) the top of the carrier's buried via. This requires creating either a solid copper through via, or a via that is filled and plated over in the carrier. Creation of such vias becomes problematic as via size and dielectric thickness decrease. In order to form a large enough via in the carrier to drill and fill effectively, the minimum producible drill-to-adjacent-feature spacing cannot be maintained. Likewise, filling a through via on a thin carrier has limited producibility due to limitations of via fill and plating processes related to decreased carrier thickness. Also, restrictions on high aspect ratio of the filled hole effectively limit the thickness of the carrier's dielectric layer. However, in certain situations a thicker dielectric layer might be required, e.g., for impedance purposes, or for overall finished dimensions of the PCB. Furthermore, thin dielectric layers, which may be required to maintain a minimum aspect ratio for μvias formed therein, may lack the necessary dimensional stability for processing, e.g., filling a plated hole, which may result in destruction of the carrier.

[0006] In addition, filling a via of the prior art usually requires multiple plating cycles, and consequently may result in unacceptably thick total surface copper for etching fine features on a signal layer. Consequently, a significant portion of the total surface copper may have to be removed by mechanical means during processing according to the prior art.

[0007] Figure 1A is a cross-sectional view of a copper clad dielectric layer 10 for processing into a conventional two-layer carrier for a PCB, according to the prior art. Copper clad dielectric layer 10 includes a first copper layer 20, a second copper layer 22, and a dielectric layer 24 disposed between first and second copper layers 20, 22. Dielectric layer 24 may comprise a dielectric material, such as a glass fiber reinforced resin, or a polyimide, and the like.

[0008] Figure 1B is a cross-sectional view of a conventional carrier 10' for a

PCB in the form of a two-layer core, according to the prior art. Carrier 10' has two metal layers, namely a first copper layer 20 and a second copper layer 22, as well as a dielectric layer 24 disposed between first and second copper layers 20, 22. Carrier 10' includes a plated through hole 40 which has been filled and plated over. Plated through hole 40 extends from a first pad 30 within first copper layer 20 to a second pad 32 within second copper layer 22. Plated through hole 40 serves as a conducting interconnection between first and second copper layers 20, 22. Such plated through holes are well known in the art. Regions of the prior art two-layer core that lack first and second copper layers 20, 22, e.g., due to etching thereof, are represented by reference numeral 26.

[0009] Figure 1C is a cross-sectional view of a conventional carrier 10'' for a PCB in the form of a two-layer core, also according to the prior art. Carrier 10'' includes a dielectric layer 24 disposed between first and second copper layers 20, 22, essentially as described for Figure 1B. Figure 1C shows a blind via 40' which has been filled and plated over. Blind via 40' extends from a first pad 30 within first copper layer 20 to a second pad 32 within second copper layer 22. Blind via 40' serves as a conducting interconnection between different layers of a multilayer PCB, e.g., between first and second copper layers 20, 22. Such blind vias are well known in the art. Regions of prior art carrier 10'' that lack first and second copper layers 20, 22, e.g., due to etching thereof, are represented by reference numeral 26.

[0010] As noted hereinabove, conventional two-layer cores of the prior art have a number of drawbacks and disadvantages. As an example, as hole size (e.g., via diameter) diminishes to accommodate higher interconnect densities, dielectric thickness must also decrease in order to maintain a certain minimum aspect ratio for the hole, since holes having aspect ratios below the producible minimum cannot be filled efficiently or reliably. Restrictions on dielectric thickness, in turn, are associated with a number of other disadvantages. However, dielectrics below a certain thickness cannot be processed reliably, leading to destruction of many incipient cores and poor processing efficiency. For example, increased dielectric thickness may be required for impedance purposes. Furthermore, a PCB having a relatively large overall dielectric thickness may offer advantages for providing connections thereto. In addition, increased overall dielectric thickness may allow for production of a PCB having a greater overall finished thickness, for example, to fit within a particular housing of an

instrument, device, or appliance.

[0011] As can be seen, there is a need for a multilayer PCB having an interlayer interconnection unit, the formation of which requires only a single plating cycle. The use of only a single plating cycle can result in decreased thickness of total surface copper, thereby facilitating formation of fine features without the need for mechanical reduction of the surface copper layer. There is also a need for a dual via interlayer interconnection unit for a multilayer PCB, wherein the interconnection unit allows an overall increased aspect ratio, as compared with prior art plated through holes and vias. There is a further need for a PCB core or subassembly wherein the total thickness of the dielectric, at minimum hole and pad diameter, can be increased when greater dielectric thickness is required, for example, for impedance purposes or for overall finished thickness.

SUMMARY OF THE INVENTION

[0012] In one aspect of the present invention, an interlayer interconnection unit for a multi-layer printed circuit board (PCB) comprises an interstitial bridge pad having a first side and a second side, wherein the interstitial bridge pad is disposed between a first dielectric layer and a second dielectric layer; a first blind via disposed on the first side of the interstitial bridge pad, wherein the first blind via extends through the first dielectric layer; and a second blind via disposed on the second side of the interstitial bridge pad, wherein the second blind via extends through the second dielectric layer.

[0013] In another aspect of the present invention, an interlayer interconnection unit for a multi-layer PCB comprises a first capture pad having a first annular ring; a first via having a first via inner end and a first via outer end, with the first via outer end in contact with the first capture pad and encircled by the first annular ring; an interstitial bridge pad having a first side and a second side, with the first via inner end in contact with the first side of the interstitial bridge pad; a second via having a second via inner end and a second via outer end, with the second via inner end in contact with the second side of the interstitial bridge pad; and a second capture pad having a second annular ring, with the second via outer end in contact with the second capture pad and encircled by the second annular ring.

[0014] In yet another aspect of the present invention, a dual blind via interconnection unit for a multilayer PCB comprises a pair of opposed coaxial blind vias; and a bridge pad disposed between the pair of blind vias, wherein each of the pair of blind vias is in contact with the bridge pad.

[0015] In still another aspect of the present invention, a carrier for a multi-layer PCB comprises a pseudo three-layer core. The pseudo three-layer core includes a first metal layer, a first dielectric layer disposed on the first metal layer, a bridge layer disposed on the first dielectric layer, a second dielectric layer disposed on the bridge layer, and a second metal layer disposed on the second dielectric layer. The bridge layer comprises a plurality of spaced apart interstitial bridge pads, and each of the plurality of interstitial bridge pads is adapted for providing an interlayer interconnection between the first metal layer and the second metal layer.

[0016] In a further aspect of the present invention, a pseudo three-layer core for a PCB may comprise a plurality of interlayer interconnection units, wherein each of the interlayer interconnection units extends from a first metal layer to a second metal layer; a first dielectric layer disposed on the first metal layer; a bridge layer disposed on the first dielectric layer; and a second dielectric layer disposed on the bridge layer, wherein the second metal layer is disposed on the second dielectric layer. Each of the interlayer interconnection units may comprise an interstitial bridge pad located within the bridge layer, a first blind via extending from the first metal layer to a first side of the interstitial bridge pad, and a second blind via extending from the second metal layer to a second side of the interstitial bridge pad.

[0017] In yet a further aspect of the present invention, a multi-layer PCB comprises a first signal layer; a second signal layer; a bridge layer disposed between the first signal layer and the second signal layer; and a plurality of interlayer interconnection units. Each of the interlayer interconnection units may be adapted for connecting the first signal layer with the second signal layer through the bridge layer.

[0018] In still a further aspect of the present invention, a multi-layer PCB comprises at least one pseudo three-layer core. Each pseudo three-layer core may include a first metal layer, a first dielectric layer disposed on the first metal layer, a bridge layer disposed on the first dielectric layer, a second dielectric layer disposed on the bridge layer, a second metal layer disposed on the second dielectric layer, and a

plurality of interlayer interconnection units. Each of the interlayer interconnection units may comprise an interstitial bridge pad having a first side and a second side, a first blind via disposed on the first side of the interstitial bridge pad, and a second blind via disposed on the second side of the interstitial bridge pad.

[0019] In an additional aspect of the present invention, a multilayer PCB may comprise a means for carrying a plurality of signal layers; and a plurality of means for interconnecting at least two of the signal layers, wherein the carrying means comprises a pseudo three-layer core, wherein the pseudo three-layer core includes an internal bridge layer, wherein the bridge layer comprises a plurality of interstitial bridge pads, and wherein each of the interconnecting means comprises a pair of opposed blind vias disposed on either side of each of the interstitial bridge pads.

[0020] In yet an additional aspect of the present invention, a method for forming a multilayer PCB comprises providing a metal clad first dielectric layer having a first metal clad side and a second metal clad side; forming a bridge layer from the second metal clad side, wherein the bridge layer comprises a plurality of bridge pads, and wherein the first metal clad side comprises a first metal layer; providing a second dielectric layer on the bridge layer, wherein the second dielectric layer has a second metal layer disposed thereon; forming a plurality of first blind vias through the first dielectric layer, with the plurality of first blind vias extending from the first metal layer to a first side of each of the plurality of bridge pads; and forming a plurality of second blind vias through the second dielectric layer, with the plurality of second blind vias extending from the second metal layer to a second side of each of the plurality of bridge pads.

[0021] In still a further aspect of the present invention, a method for forming a multilayer PCB comprises forming a pseudo three-layer core, wherein the pseudo three-layer core includes a first metal layer, a first dielectric layer disposed on the first metal layer, a bridge layer disposed on the first dielectric layer, a second dielectric layer disposed on the bridge layer, and a second metal layer disposed on the second dielectric layer, wherein the bridge layer comprises a plurality of spaced apart interstitial bridge pads. The method further comprises forming a plurality of interlayer interconnection units for interconnecting the first metal layer and the second metal layer, wherein each of the interlayer interconnection units includes a first blind via disposed on a first side of one of the plurality of interstitial bridge pads, wherein the first blind via extends from

the first metal layer through the first dielectric layer; and a second blind via disposed on a second side of one of the plurality of interstitial bridge pads, wherein the second blind via extends from the second metal layer through the second dielectric layer.

[0022] In yet an additional aspect of the present invention, a method for forming a multilayer PCB comprises a step for forming a pseudo three-layer core, wherein the pseudo three-layer core includes a first metal layer, a first dielectric layer disposed on the first metal layer, a bridge layer disposed on the first dielectric layer, a second dielectric layer disposed on the bridge layer, and a second metal layer disposed on the second dielectric layer, wherein the bridge layer comprises a plurality of bridge pads. The method further comprises a step for forming a plurality of interlayer interconnection units for interconnecting the first metal layer and the second metal layer, wherein each of the interlayer interconnection units includes a first blind via disposed on a first side of one of the plurality of interstitial bridge pads, wherein the first blind via extends from the first metal layer through the first dielectric layer, and a second blind via disposed on a second side of one of the plurality of interstitial bridge pads, wherein the second blind via extends from the second metal layer through the second dielectric layer.

[0023] In still another aspect of the present invention, a method for forming a pseudo three-layer core for a PCB comprises providing a first metal layer; providing a first dielectric layer on the first metal layer; forming a bridge layer on the first dielectric layer, wherein the bridge layer comprises a plurality of bridge pads; providing a second dielectric layer on the bridge layer; providing a second metal layer on the second dielectric layer; forming a first blind via on a first side of each of the plurality of bridge pads, wherein the first blind via extends from the first metal layer through the first dielectric layer; and forming a second blind via on a second side of each of the plurality of bridge pads, wherein the second blind via extends from the second metal layer through the second dielectric layer.

[0024] These and other features, aspects, and advantages of the present invention will become better understood with reference to the following drawings, description, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Figure 1A is a cross-sectional view of a copper clad dielectric layer for processing into a conventional two-layer carrier for a printed circuit board (PCB), according to the prior art;

[0026] Figure 1B is a cross-sectional view of a conventional carrier for a PCB in the form of a two-layer core having a plated through hole therein, also according to the prior art;

[0027] Figure 1C is a cross-sectional view of a conventional carrier for a PCB in the form of a two-layer core having a blind via therein, also according to the prior art;

[0028] Figure 2 is a block diagram schematically representing a multilayer PCB having at least one carrier comprising a pseudo three-layer core, according to one embodiment of the present invention;

[0029] Figure 3 schematically represents a plurality of interlayer interconnection units within a portion of a pseudo three-layer core, as seen in sectional view, according to one embodiment of the present invention;

[0030] Figure 4A is a perspective view of an interlayer interconnection unit within a pseudo three-layer core, according to one embodiment of the present invention;

[0031] Figure 4B is a side view of the interlayer interconnection unit of Figure 4A, according to the present invention;

[0032] Figure 5 is a plan view of a portion of a bridge layer of a carrier for a multilayer PCB, according to one embodiment of the present invention;

[0033] Figure 6 schematically represents a carrier for a multilayer PCB having additional conductive layers on a pseudo three-layer core, according to one embodiment of the present invention;

[0034] Figure 7 schematically represents a series of steps involved in a method for making a conventional carrier for a multilayer PCB, according to the prior art;

[0035] Figure 8 schematically represents a series of steps involved in a method for making a multilayer PCB, according to another embodiment of the present invention;

[0036] Figure 9 schematically represents a series of steps involved in a method for making a multilayer PCB, according to yet another embodiment of the present invention;

[0037] Figure 10 schematically represents a series of steps involved in a method

for making a carrier for a multilayer PCB, according to a further embodiment of the present invention; and

[0038] Figures 11A-E illustrate stages in a process for forming an interlayer interconnection unit for a multilayer PCB, according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0039] The following detailed description is of the best currently contemplated modes of carrying out the invention. The description is not to be taken in a limiting sense, but is made merely for the purpose of illustrating the general principles of the invention, since the scope of the invention is best defined by the appended claims.

[0040] Generally, the present invention provides a carrier for a multilayer printed circuit board (PCB) or printed wiring board, wherein the carrier may include a novel interlayer interconnection unit for interconnecting a plurality of conductive layers of the multilayer PCB. A basic carrier, sub-assembly, or building block according to one embodiment of the invention may comprise a pseudo three-layer core. Each pseudo three-layer core may comprise two signal layers for a multilayer PCB, wherein the two signal layers are interconnected through an interconnection unit comprising an internal bridge layer disposed between the two signal layers.

[0041] A pseudo three-layer core of the present invention may have additional layers added thereto. For example, a multilayer PCB of the invention may comprise a single pseudo three-layer core, and up to six (6) or more conductive layers. A plurality of carriers may be combined, e.g., laminated together, to form a multilayer PCB having up to about 28 or more signal layers. Multilayer PCBs find almost universal applications in electrical or electronic devices, instruments, and appliances.

[0042] In contrast to a conventional two-layer core of the prior art, for example, as described hereinabove with reference to Figures 1B-C, in one embodiment the present invention provides a carrier having two dielectric layers, a bridge layer disposed between the two dielectric layers, and a pair of external conductive layers. As compared with carriers of the present invention, prior art carriers, i.e., two-layer cores of prior art multilayer PCBs, have only a single dielectric layer and lack a bridge layer. As compared with prior art multilayer PCBs which have a carrier comprising a two-layer core in which a single dielectric layer is disposed between two conductive layers,

multilayer PCBs of the present invention have a carrier comprising a three-layer core, or pseudo three-layer core, including a pseudo metal layer or bridge layer disposed between two dielectric layers.

[0043] The bridge layer of carriers of the present invention may be referred to as a pseudo metal layer in that the bridge layer is not a metal layer of the type encountered in prior art carriers, for example, due to the lack of electrical connectivity within the bridge layer between the metal bridge pads that constitute the bridge layer. Due to the presence of the internal pseudo metal (bridge) layer in carriers of the present invention, the basic carrier of the invention, which may comprise the bridge layer, the two dielectric layers, and the pair of external conductive layers, may be referred to as a pseudo three-layer core. The pair of outer conductive layers may be interconnected by a plurality of interlayer interconnection units, wherein each interconnection unit may comprise an interstitial bridge pad located within the bridge layer, and a pair of coaxial, opposed blind vias disposed on either side of the interstitial bridge pad.

[0044] In some embodiments of the present invention, a pseudo three-layer core of the invention may itself constitute a multilayer PCB. In other embodiments of the invention, additional dielectric layers and additional conductive (e.g., signal) layers may be sequentially laminated to the pseudo three-layer core. Furthermore, two or more pseudo three-layer cores of the present invention, with or without additional dielectric and conductive layers, may be laminated to each other to form multilayer PCBs having up to 28 or more signal layers.

[0045] Figure 2 is a block diagram schematically representing a multilayer PCB 100, according to one embodiment of the present invention. Multilayer PCB 100 may include a first carrier or core 110a. In some embodiments, multilayer PCB 100 may further include one or more additional carriers 110n. The one or more additional carriers 110n may be laminated to first carrier 110a. Each of first carrier 110a and additional carrier(s) 110n may comprise a pseudo three-layer core of the present invention. Each pseudo three-layer core may comprise two signal layers. Such a pseudo three-layer core is described fully hereinbelow, for example, with respect to Figures 4A-B. In some embodiments, one or more of first carrier 110a and additional carriers 110n may further comprise one or more additional signal layers 120', 122' (Figure 6).

[0046] Figure 3 is a sectional view showing a plurality of interlayer interconnection units within a portion of a pseudo three-layer core 110, according to an embodiment of the present invention. Pseudo three-layer core 110 may include a first interlayer interconnection unit 150a, and an n^{th} interlayer interconnection unit 150n. Pseudo three-layer core 110 may include a first metal layer 120, a first dielectric layer 124 disposed on first metal layer 120, a bridge layer 126 disposed on first dielectric layer 124, a second dielectric layer 125 disposed on bridge layer 126, and a second metal layer 122 disposed on second dielectric layer 125. Each of interlayer interconnection units 150a and 150n extend from first metal layer 120, through bridge layer 126, to second metal layer 122. For the purpose of clarity, only two interconnection units 150a, 150n are shown in Figure 3. In practice, pseudo three-layer core 110 may include any number of interlayer interconnection units. Typically, interlayer interconnection units 150a, 150n may be present only at locations, with respect to the x and y dimensions of a PCB, at which it is desired to interconnect first metal layer 120 to second metal layer 122. Locations at which interlayer interconnection units 150a, 150n may be present correspond to the locations of bridge pads 134. Such locations of bridge pads 134 are schematically represented in Figure 5. The x and y dimensions are shown in Figure 5 by the arrows labeled "x" and "y" respectively. Interlayer interconnection units of the present invention are further described hereinbelow, e.g., with reference to Figures 4A-B.

[0047] Figure 4A shows an interlayer interconnection unit 150 within a three-layer core 110, with interlayer interconnection unit 150 shown in perspective view, according to one embodiment of the present invention. Three-layer core 110 may include an internal bridge layer 126 disposed between first dielectric layer 124 and second dielectric layer 125. Three-layer core 110 may further include first and second metal layers 120, 122, respectively, as described hereinabove.

[0048] Bridge layer 126 may comprise a plurality of spaced apart interstitial bridge pads 134. Each bridge pad 134 may comprise an essentially disc-shaped conductive element, e.g., a copper disc. Each bridge pad 134 may lack electrical connection to other bridge pads 134 within bridge layer 126. Interlayer interconnection unit 150 may include one bridge pad 134 located within bridge layer 126 (Figure 5).

That is to say, each bridge pad 134 may be a component of an interlayer interconnection unit 150.

[0049] Interlayer interconnection unit 150 may further include a first capture pad 130 within first metal layer 120, and a second capture pad 132 within second metal layer 122. First capture pad 130 and second capture pad 132 may each comprise a conductive (e.g., copper) element, which may be formed by the selective removal, e.g., by etching, of first metal layer 120 and second metal layer 122, respectively. It is apparent from Figure 4A that bridge pad 134 may have a diameter, D_b that is greater than a diameter, D_c of first and second capture pads 130, 132. First Interlayer interconnection unit 150 may still further include a first blind via 140 and a second blind via 142. Each of first blind via 140 and second blind via 142 may be formed by a process such as laser drilling, plasma drilling, or photo-definition (photo-defining). Although Figure 4A shows a gap 112 within bridge layer 126 on either side of bridge pad 134, during lamination first and second dielectric layers 124, 125 may fuse together such that bridge pad 134 may be encapsulated within first and second dielectric layers 124, 125.

[0050] During formation of interlayer interconnection unit 150, a first annular ring 131 may be formed within first metal layer 120. As an example, first annular ring 131 may comprise an annular, outer portion of first capture pad 130. Similarly, during formation of interlayer interconnection unit 150, a second annular ring 133 may be defined within second metal layer 122. As an example, second annular ring 133 may comprise an annular, outer portion of second capture pad 132. Each of first annular ring 131 and second annular ring 133 may comprise an annular conductive (e.g., copper) element.

[0051] After forming first and second blind vias 140, 142, respectively, first and second blind vias 140, 142 may be plated shut. In some embodiments, first and second blind vias 140, 142 may be plated shut using a μfill process, such as the MicroFill™ VF process of the Shipley Company, LLC (Marlborough, MA). Briefly, MicroFill™ VF is a direct current electrolytic copper plating process for filling blind vias, including μvias. (See, for example, *MicroFill™ VF, Electrolytic Copper Plating Technology for Filling Blind Microvias in HDI/Build-up Printed Wiring Boards*, Ref. No. PM02N006, Rev. No. 0, Copyright, 2002, Shipley Company, LLC (Marlborough, MA); and *MicroFill VF Process Manual,* Ref. No. PM03N002, Rev. No. 0, February, 2003, Shipley Company,

LLC (Marlborough, MA), both of which are incorporated by reference herein).

[0052] Figure 4B is a side view of the interlayer interconnection unit of Figure 4A, according to the present invention. First and second dielectric layers 124, 125 are omitted from Figure 4B for the sake of clarity. As may be seen in Figures 4A-B, bridge pad 134 may include a first side 134a and a second side 134b. First blind via 140 may include a first via inner end 140a and a first via outer end 140b. Inner end 140a may be in electrical contact with bridge pad first side 134a, while outer end 140b may be in electrical contact with first capture pad 130 and encircled by first annular ring 131. Second blind via 142 may include a second via inner end 142a and a second via outer end 142b. Inner end 142a may be in electrical contact with bridge pad second side 134b, while outer end 142b may be in electrical contact with second capture pad 132 and encircled by second annular ring 133. First and second annular rings 131, 133, may be considered to be the remaining annular portion of first and second capture pads 130, 132, respectively, after formation of a hole therethrough. Thus, interlayer interconnection unit 150 may extend from first capture pad 130, through first blind via 140, bridge pad 134, second blind via 142, and thence to second capture pad 132.

[0053] Again with reference to Figures 4A-B, each of first and second blind vias 140, 142, respectively, may have an aspect ratio of about 1:1, and usually at least about 1:1. Because first and second blind vias 140, 142 are aligned in the z dimension, or coaxial with each other, interlayer interconnection unit 150 may have an effective aspect ratio of about 2:1, and often greater than 2:1. Thus, interlayer interconnection unit 150 of the instant invention allows for a greater than two fold (2X) increase in effective aspect ratio for interconnecting adjacent conductive layers of multilayer PCBs, as compared with the prior art. At the same time, because pseudo three-layer core 110 of the instant invention has two dielectric layers and two signal layers (as compared with only one dielectric layer in prior art two-layer cores) the total dielectric thickness (i.e., the combined thickness of first and second dielectric layers 124, 125) per signal layer (e.g., the mean thickness of first metal layer 120 and second metal layer 122) may be increased by about two fold in carriers of the present invention as compared with a prior art two-layer core. This increase in total dielectric thickness per signal layer is achieved without increasing the aspect ratio of each blind via, i.e., of first and second blind vias 140, 142. The effective aspect ratio of interlayer interconnection unit 150, as referred to herein, is the ratio of the length, L (Figure 4B) (i.e., the z dimension) of interlayer

interconnection unit 150 to the diameter, D_v (Figure 4B) of first and second blind vias 140, 142. The z axis is indicated in Figure 4A by the vertical arrow labeled "z".

[0054] Figure 5 is a plan view of a portion of a bridge layer 126 of a carrier for a multilayer PCB of the present invention. Bridge layer 126 may include a plurality of interstitial bridge pads 134. Each interstitial bridge pad 134 may comprise a metal, such as copper. The plurality of interstitial bridge pads 134 may be conveniently formed by etching one side of a copper clad dielectric layer 124 (e.g., Figures 11A-B).

[0055] Interstitial bridge pads 134 may be spaced apart from each other by a distance, S in the range of from about 0.7 to 4 mils, with a center-to-center pitch, P in the range of from about 15 to 25 mils. Each interstitial bridge pad 134 may have a diameter, d in the range of from about 12 to 20 mils, usually in the range of from about 14 to 17 mils, and often in the range of from about 15 to 16 mils. Interstitial bridge pads 134 typically lack electrical connectivity, within bridge layer 126, to other bridge pads 134, or to any other conductive element (e.g., a trace or a component) of bridge layer 126. That is to say, bridge layer 126 may consist of a plurality of spaced apart bridge pads 134, with no electrical connections therebetween within bridge layer 126.

[0056] Figure 6 schematically represents a carrier 110' for a multilayer PCB, according to one embodiment of the present invention. Carrier 110' may include a pseudo three-layer core 110. As shown, carrier 110' may further include a first additional dielectric layer 124' and a first additional conductive layer 120' laminated thereto. Carrier 110' may still further include a second additional dielectric layer 125' and a second additional conductive layer 122' laminated thereto. In other embodiments of the invention (not shown in Figure 6), carrier 110' may have fewer or more additional dielectric and conductive layers than those shown in Figure 6 laminated to pseudo three-layer core 110.

[0057] As described hereinabove, pseudo three-layer core 110 may itself comprise two signal layers 120, 122. By adding additional conductive layers, e.g., layers 120', 122' to pseudo three-layer core 110, each carrier 110' may comprise from three to six or more conductive layers (only four conductive layers 120, 122, 120', and 122' are shown in Figure 6). Each of layers 120, 122, 120', and 122', or of any other additional conductive layers (not shown in Figure 6) of a carrier or multilayer PCB 100 may comprise a signal layer; or one or more conductive layers (e.g., layers 120, 122, 120', and 122', or other additional conductive layers) of a carrier or multilayer PCB 100

may comprise a plane or ground layer, as is well known in the art. Two or more carriers 110' may be combined (laminated) together (Figure 2) to form a multilayer PCB having from four to 28 or more conductive layers (see, e.g., Figure 6).

[0058] Figure 7 schematically represents a series of steps (202-214) involved in a method 200 for making a conventional carrier for a multilayer PCB, according to the prior art. Step 202 involves providing a metal clad dielectric layer, such as a layer of dielectric material having a layer of copper foil on each side. Due to production limitations associated with filling μvias of a defined diameter and aspect ratio in a thin dielectric layer, the minimum thickness of the dielectric layer in prior art PCBs is typically about 4 mils.

[0059] Step 204 involves forming pads (capture pads and target pads) on the copper layers by etching the copper foil. The formation of such pads is well known in the art. Due to the industry trend towards high-density interconnections, the diameter of current state of the art capture pads and target pads is typically limited to around 10 mils. In prior art processing, there may be difficulties in aligning the drill to pads of this size. In comparison, bridge pads 134 of the invention may have diameters, d up to about 20 mils or more. The larger diameter, d f bridge pads 134 of the invention is possible because the pseudo metal layer (or bridge layer) 126 of carriers of the invention may lack traces, components, or other conductive features. The larger diameter of bridge pads 134 of the invention offer the advantage of facilitating drill registration during via formation.

[0060] Step 206 involves drilling a hole though one or both of the copper layers and the dielectric layer, to form a blind via or a through hole. Step 208 involves plating the hole. Thereafter, step 208, which entails a first plating cycle of the prior art process, adds to the overall thickness of the surface copper. Step 210 involves filling the hole with electrically conductive material, such as a high solids epoxy. Filling the hole in this manner becomes impracticable for presently used dielectric thickness, hole diameter, and aspect ratio. Step 212 involves plating over the fill, in a second plating cycle, to provide a contiguous metal layer over the filled hole. Thus, step 212 further adds to the surface copper thickness.

[0061] Excessive thickness of surface copper may prevent etching of fine features. For example, for a PCB having a 3 mil line and space specification, a surface copper thickness of 1.4 mils or less may be required. Prior art processes that result in

surface copper thickness greater than 1.4 mils may require additional processing steps to remove excess surface copper.

[0062] Step 214 of the prior art process involves planarizing the copper layer(s) in which holes have been drilled, plated, filled, and plated over. Planarizing may be accomplished by mechanical reduction of surface copper, which process may excessively stress the carrier. In situations, where surface copper exceeds the maximum permissible thickness, reduction of surface copper may damage or destroy the carrier or its components, leading to decreased manufacturing efficiency.

[0063] In contrast to the prior art, processes of the invention for making a multilayer PCB may use only one plating cycle. As a result, a total surface copper thickness of about 1 mil or less can be readily achieved. Lower total surface copper thickness decreases the amount of planarizing and mechanical reduction of surface copper, and allows finer line and space resolution.

[0064] Figure 8 schematically represents a series of steps (302-318) which may be involved in a method 300 for making a multilayer PCB, according to one embodiment of the present invention. Step 302 may involve providing a metal clad first dielectric layer, such as a dielectric layer having a first side and a second side, and a layer of copper foil on both the first side and the second side. Step 304 may involve forming a bridge layer on one side of the dielectric layer. The bridge layer may comprise a plurality of spaced apart bridge pads, as described herein (Figures 4A-B, Figure 5). The bridge layer may be formed by etching the copper foil on one side of the dielectric layer. Alternatively, the bridge pads and the bridge layer may be formed by building up from an exposed dielectric layer using an additive technology. The bridge layer formed during step 302 may be referred to as a pseudo metal layer.

[0065] Step 306 may involve providing a second dielectric layer disposed on the bridge layer. Step 308 may involve providing a second metal layer laminated to the second dielectric layer. Steps 306 and 308 may be combined into a single process in which a dielectric layer, which has been clad with the second metal layer, may be disposed on the bridge layer.

[0066] Step 310 may involve forming a first blind via, wherein the first blind via extends from the first metal layer, through the first dielectric layer, and to a first side of a bridge pad within the bridge layer. Step 312 may involve forming a second blind via

from the second metal layer, through the second dielectric layer, and to a second side of the bridge pad within the bridge layer. Each of the first blind via and the second blind via 142 may be formed by a process such as laser drilling, plasma drilling, or photo-defining. Typically, the first blind via may emanate from a first capture pad of the first metal layer, and the second blind via may emanate from a second capture pad of the second metal layer. The first and second capture pads may be formed by etching the first and second metal layers, respectively.

[0067] Step 314 may involve plating shut the first and second blind vias, such that an interlayer interconnection unit may be formed within a multilayer carrier, wherein the interlayer interconnection unit may include a bridge pad disposed between the first and second blind vias (Figure 4A). The first and second blind vias may be opposed to each other in the z dimension and coaxial with the bridge pad. The first and second blind vias may be plated shut in a single plating cycle using a μfill process, such as the MicroFill™ VF process of the Shipley Company, LLC (Marlborough, MA), as referred to hereinabove.

[0068] Optional step 316 may involve laminating one or more additional dielectric layers, and one or more additional metal layers, to the first and second metal layers of the basic carrier or pseudo three-layer core formed by steps 302-314. In this way, a carrier having up to six or more signal layers may be formed. Optional step 318 can involve laminating together two or more carriers formed by steps 302-314, or by steps 302-316, to provide a multilayer PCB having from 4 to 28 or more signal layers.

[0069] Figure 9 schematically represents a series of steps (402-404) involved in a method 400 for making a multilayer PCB, according to another embodiment of the present invention. Step 402 may involve forming a multilayer carrier or a pseudo three-layer core. A pseudo three-layer core formed according to step 402 may include two signal layers. In some embodiments, the multilayer carrier or pseudo three-layer core may be considered to be a sub-assembly for the multilayer PCB. For example, additional signal layers may be laminated to the pseudo three-layer core; or two or more pseudo three-layer cores may be laminated together to form a multilayer PCB having at least 4 signal layers. Step 404 may involve forming a plurality of interlayer interconnection units within the carrier for interconnecting two or more conductive layers of the carrier. Interlayer interconnection units of the invention were described hereinabove (e.g., with reference to Figures 4A-B). Formation of interlayer

interconnection units of the invention is also described herein, for example, with reference to method 400 (Figure 9).

[0070] Figure 10 schematically represents a series of steps (502-514) involved in a method 500 for making a carrier for a multilayer PCB, according to another embodiment of the present invention, wherein step 502 may involve providing a first metal layer. Step 504 may involve providing a first dielectric layer. The first metal layer may be laminated to a first side of the first dielectric layer.

[0071] Step 506 may involve forming a bridge layer. Bridge layer, which may comprise a plurality of spaced apart bridge pads, may be formed by etching a layer of copper foil laminated to a second side of the first dielectric layer. Formation of the bridge layer is described elsewhere herein, for example, with reference to method 200 (Figure 7).

[0072] Step 508 may involve providing a second dielectric layer. The second dielectric layer provided in step 508 may be laminated to the bridge layer, such that the bridge pads of bridge layer are encapsulated in dielectric material between the first and second dielectric layers. Step 510 may involve providing a second metal layer, which may be laminated to the second dielectric layer.

[0073] Step 512 may involve forming a first blind via of an interlayer interconnection unit, wherein the first blind via may be disposed between the first metal layer and a first side of a bridge pad. Step 514 may involve forming a second blind via of the interlayer interconnection unit, wherein the second blind via may be disposed between the second metal layer and a second side of the bridge pad. First and second blind vias formed on opposite sides of a bridge pad within a multilayer carrier are described hereinabove, e.g., with reference to Figures 4A-B and Figure 7.

[0074] In method 500, first and second blind vias may be plated shut in a single plating cycle, for example, as described with reference to method 200 (Figure 7). Use of a single plating cycle minimizes excessive build-up of surface copper, and therefore decreases the need for subsequent reduction of surface copper, as described hereinabove. Optionally, after forming and plating shut the first and second blind vias to form a pseudo three-layer core, one or more additional dielectric layers and metal layers may be laminated to the pseudo three-layer core (see, e.g., step 316 of method 300 (Figure 8)).

[0075] Figures 11A-E illustrate stages in forming an interlayer interconnection

unit for a multilayer PCB, according to one embodiment of the present invention. Figure 11A shows a first dielectric layer 124 which can be clad on each side with a layer of copper foil, namely a first layer of copper foil 120 and a second layer of copper foil 126'. First dielectric layer 124 may also be referred to as a metal clad first dielectric layer 124 having a first metal clad side clad with a first layer of copper foil 120, and a second metal clad side clad with a second layer of copper foil 126'. The first layer of copper foil 120 may also be referred to herein as first metal layer 120. The second layer of copper foil 126' may be etched to form a bridge layer 126 (Figures 11B-E).

[0076] Figure 11B shows a bridge pad 134, which may be formed by etching second layer of copper foil 126'. For the sake of clarity, Figures 11B-E show only one bridge pad 134 within bridge layer 126; however in practice, a much larger number of bridge pads may be formed within bridge layer 126.

[0077] Figure 11C shows the structure of Figure 11B and which may have a second dielectric layer 125 and a second metal layer 122 laminated thereto. Although Figures 11C-E show a gap 112 within bridge layer 126 adjacent to bridge pad 134, during lamination first and second dielectric layers 124, 125 may fuse around bridge pad 134 such that bridge pad 134 may be encapsulated within first and second dielectric layers 124, 125.

[0078] Figure 11D illustrates the structure of Figure 11C after etching first and second metal layers 120, 122, respectively to form capture pads 130, 132, respectively. Figure 11 D also shows a first blind via 140 and a second blind via 142. First and second blind vias 140, 142 can extend from first and second metal layers 120, 122, respectively, to first and second sides of bridge pad 134.

[0079] Figure 11E shows the structure of Figure 11D which may have solid first and second blind vias 140', 142' filled and plated shut to form interlayer interconnection unit 150 for interconnecting first and second metal layers 120, 122. An interlayer interconnection unit 150 of the invention has been described hereinabove. Briefly, interlayer interconnection unit 150 may include first capture pad 130, solid first blind via 140', bridge pad 134, solid second blind via 142', and second capture pad 132.

[0080] It should be understood, of course, that the foregoing relates to preferred embodiments of the invention and that modifications may be made without departing from the spirit and scope of the invention as set forth in the following claims.

CLAIMS

1. An interlayer interconnection unit for a printed circuit board (PCB), comprising:

an interstitial bridge pad having a first side and a second side, wherein said interstitial bridge pad is disposed between a first dielectric layer and a second dielectric layer;

a first blind via disposed on said first side of said interstitial bridge pad, wherein said first blind via extends through said first dielectric layer; and

a second blind via disposed on said second side of said interstitial bridge pad, wherein said second blind via extends through said second dielectric layer, wherein said interstitial bridge pad is adapted to electrically connect said first blind via to said second blind via.

2. The interlayer interconnection unit of claim 1, wherein said interstitial bridge pad comprises a disc-shaped conductive element.

3. The interlayer interconnection unit of claim 1, wherein:

said first blind via extends from a first conductive layer, through said first dielectric layer, and to said first side of said interstitial bridge pad, and

said second blind via extends from a second conductive layer, through said second dielectric layer, and to said second side of said interstitial bridge pad.

4. The interlayer interconnection unit of claim 1, wherein said first conductive layer and said second conductive layer each comprise copper foil.

5. The interlayer interconnection unit of claim 1, wherein:

said first blind via extends from a first capture pad to said first side of said interstitial bridge pad, and

said second blind via extends from a second capture pad to said second side of said interstitial bridge pad.

6. The interlayer interconnection unit of claim 5, wherein said first capture

pad and said second capture pad each have a diameter less than a diameter of said interstitial bridge pad.

7. The interlayer interconnection unit of claim 1, wherein said interstitial bridge pad has a diameter in the range of from about 12 to 20 mils.

8. The interlayer interconnection unit of claim 1, wherein:

said PCB comprises a bridge layer disposed between said first dielectric layer and said second dielectric layer, and

said interstitial bridge pad is located within said bridge layer, and wherein said interstitial bridge pad lacks electrical connection, within said bridge layer, to a conductive element of said bridge layer.

9. The interlayer interconnection unit of claim 1, wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via.

10. An interlayer interconnection unit for a multi-layer PCB, comprising:

a first capture pad having a first annular ring;

a first via having a first via inner end and a first via outer end, said first via outer end in contact with said first capture pad and encircled by said first annular ring;

an interstitial bridge pad having a first side and a second side, said first via inner end in contact with said first side of said interstitial bridge pad;

a second via having a second via inner end and a second via outer end, said second via inner end in contact with said second side of said interstitial bridge pad; and

a second capture pad having a second annular ring, said second via outer end in contact with said second capture pad and encircled by said second annular ring.

11. The interconnection unit of claim 10, wherein said first annular ring, said first via, said interstitial bridge pad, said second via, and said second annular ring are coaxial with each other.

12. The interconnection unit of claim 10, wherein:
said first via extends through a first dielectric layer, and
said second via extends through a second dielectric layer.

13. The interconnection unit of claim 10, wherein said interstitial bridge pad has a diameter in the range of from about 14 to 17 mils.

14. The interconnection unit of claim 10, wherein:
said multilayer PCB comprises an internal bridge layer, and
said interstitial bridge pad is a component of said bridge layer.

15. The interconnection unit of claim 10, wherein each of said first via and said second via has an aspect ratio of at least about 1:1.

16. The interconnection unit of claim 10, wherein said interconnection unit has an effective aspect ratio greater than about 2:1.

17. The interconnection unit of claim 10, wherein:
said first capture pad is located within a first conductive layer,
said second capture pad is located within a second conductive layer, and
said interconnection unit further comprises a third via extending from said first capture pad or said second capture pad to a third conductive layer.

18. A dual blind via interconnection unit for a multilayer PCB, comprising:
a pair of opposed coaxial blind vias; and
a bridge pad disposed between said pair of blind vias, wherein each of said pair of blind vias is in contact with said bridge pad, and wherein said bridge pad is adapted to electrically interconnect said pair of opposed coaxial blind vias.

19. The interconnection unit of claim 18, wherein said bridge pad has a diameter in the range of from about 12 to 20 mils.

20. The interconnection unit of claim 19, wherein each of said pair of blind vias has a diameter in the range of from about 4 to 6 mils.

21. A carrier for a multi-layer printed circuit board (PCB), said carrier comprising a pseudo three-layer core, said pseudo three-layer core including:

a first metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer; and

a second metal layer disposed on said second dielectric layer,

wherein said bridge layer comprises a plurality of spaced apart interstitial bridge pads, and

wherein at least one of said plurality of interstitial bridge pads is adapted for providing an interlayer interconnection between said first metal layer and said second metal layer.

22. The carrier of claim 21, wherein:

each of said plurality of interstitial bridge pads is connected to said first metal layer by a first blind via, and

each of said plurality of interstitial bridge pads is connected to said second metal layer by a second blind via.

23. The carrier of claim 21, wherein said bridge layer lacks an electrical connection between said plurality of interstitial bridge pads.

24. The carrier of claim 21, wherein said plurality of interstitial bridge pads are spaced apart from each other by a distance in the range of from about 0.7 to 4 mils.

25. The carrier of claim 24, wherein said plurality of interstitial bridge pads are arranged within said bridge layer at a center-to-center pitch in the range of from about 15 to 25 mils.

26. The carrier of claim 21, wherein:

said first metal layer comprises a first signal layer of said PCB, and

said second metal layer comprises a second signal layer of said PCB.

27. The carrier of claim 26, further comprising at least a third signal layer laminated to said pseudo three-layer core.

28. The carrier of claim 26, wherein said carrier comprises from 2 to 4 additional signal layers laminated to said pseudo three-layer core.

29. A pseudo three-layer core for a printed circuit board (PCB), comprising:

a plurality of interlayer interconnection units, wherein each of said plurality of interlayer interconnection units extends from a first metal layer to a second metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer; and

a second dielectric layer disposed on said bridge layer,

wherein said second metal layer is disposed on said second dielectric layer, and

wherein at least one of said plurality of interlayer interconnection units comprises:

an interstitial bridge pad located within said bridge layer;

a first blind via extending from said first metal layer to a first side of said interstitial bridge pad; and

a second blind via extending from said second metal layer to a second side of said interstitial bridge pad.

30. A multi-layer printed circuit board (PCB), comprising:

a first signal layer;

a second signal layer;

a bridge layer disposed between said first signal layer and said second signal layer; and

a plurality of interlayer interconnection units, each of said plurality of interlayer interconnection units adapted for connecting said first signal layer with said second signal layer through said bridge layer, wherein at least one said plurality of interlayer

interconnection units comprises:

a pair of opposed coaxial blind vias; and

a bridge pad disposed between, and in electrical contact with, said pair of blind vias.

31. The multi-layer PCB of claim 30, wherein:

said bridge pad includes a first side and a second side; and wherein

said pair of opposed coaxial blind vias comprise a first blind via disposed on said first side of said bridge pad, and a second blind via disposed on said second side of said bridge pad.

32. The multi-layer PCB of claim 30, further comprising at least one additional dielectric layer laminated to said first signal layer, and at least one additional signal layer laminated to said at least one additional dielectric layer.

33. A multi-layer PCB, comprising:

at least one pseudo three-layer core including:

a first metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer;

a second metal layer disposed on said second dielectric layer; and

a plurality of interlayer interconnection units for electrically interconnecting said first metal layer with said second metal layer, wherein at least one of said plurality of interlayer interconnection units comprises:

an interstitial bridge pad having a first side and a second side;

a first blind via disposed on said first side of said interstitial bridge pad; and

a second blind via disposed on said second side of said interstitial bridge pad.

34. The multilayer PCB of claim 33, wherein each of said plurality of

interlayer interconnection units is adapted for electrically interconnecting said first metal layer with said second metal layer.

35. The multilayer PCB of claim 33, wherein:

each of said first metal layer and said second metal layer comprises a signal layer, and

said multilayer PCB further comprises at least one additional signal layer laminated to said at least one pseudo three-layer core.

36. The multilayer PCB of claim 33, wherein said at least one pseudo three-layer core comprises a first pseudo three-layer core and at least a second pseudo three-layer core laminated to said first pseudo three-layer core.

37. The multilayer PCB of claim 33, wherein said multilayer PCB comprises from 1 to 4 pseudo three-layer cores and from 4 to 28 signal layers.

38. A multilayer PCB, comprising:

means for carrying a plurality of signal layers; and

means for interconnecting at least two of said plurality of signal layers,

wherein said carrying means comprises a pseudo three-layer core,

wherein said pseudo three-layer core includes an internal bridge layer that comprises a plurality of interstitial bridge pads, and

wherein said interconnecting means comprises a pair of opposed blind vias disposed on either side of each of said plurality of interstitial bridge pads.

39. The multilayer PCB of claim 38, wherein:

said bridge layer comprises an internal pseudo metal layer disposed between a first dielectric layer and a second dielectric layer, and

wherein said interconnecting means is adapted for interconnecting said plurality of signal layers.

40. A method for forming a multilayer printed circuit board (PCB), comprising:

a) providing a metal clad first dielectric layer having a first metal clad side and a second metal clad side;

b) forming a bridge layer from said second metal clad side, wherein said bridge layer comprises a plurality of bridge pads, and wherein said first metal clad side comprises a first metal layer;

c) providing a second dielectric layer on said bridge layer, wherein said second dielectric layer has a second metal layer disposed thereon;

d) forming a first blind via through said first dielectric layer, wherein said first blind via extends from said first metal layer to a first side of at least one of said plurality of bridge pads; and

e) forming a second blind via through said second dielectric layer, wherein said second blind via extends from said second metal layer to a second side of said at least one of said plurality of bridge pads.

41. The method of claim 40, wherein said step b) comprises etching said second metal clad side of said first dielectric layer to form said at least one of said plurality of bridge pads.

42. The method of claim 40, wherein:

said second metal clad side comprises copper foil, and

wherein said at least one of said plurality of bridge pads comprises copper.

43. The method of claim 40, wherein each of said plurality of bridge pads has a diameter in the range of from about 12 to 20 mils.

44. The method of claim 40, wherein said bridge layer lacks electrical connectivity between said plurality of bridge pads.

45. The method of claim 40, wherein said steps c) and d) respectively comprise forming said first blind via and said second blind via by a process selected from the group consisting of laser drilling, plasma drilling, and photo-defining.

46. The method of claim 40, further comprising:

e) plating shut said first blind via and said second blind via.

47. The method of claim 40, wherein said method involves only a single plating cycle.

48. The method of claim 46, wherein after said step e), said first metal layer and said second metal layer each have a thickness in the range of from about 0.8 to 1.4 mils.

49. The method of claim 46, wherein after said step e) said first metal layer and said second metal layer each have a thickness in the range of from about 0.9 to 1.1 mils.

50. The method of claim 40, wherein said first blind via and said second blind via each comprise a μvia having a diameter in the range of from about 4 to 5 mils.

51. A method for forming a multilayer printed circuited board (PCB), comprising:

a) forming a pseudo three-layer core, said pseudo three-layer core including:

a first metal layer;

a first dielectric layer disposed on said first metal layer,

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer; and

a second metal layer disposed on said second dielectric layer, wherein said bridge layer comprises a plurality of spaced apart interstitial bridge pads; and

b) forming a plurality of interlayer interconnection units for interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes:

a first blind via disposed on a first side of one of said plurality of interstitial bridge pads, wherein said first blind via extends from said first metal layer

through said first dielectric layer; and

a second blind via disposed on a second side of one of said plurality of interstitial bridge pads, wherein said second blind via extends from said second metal layer through said second dielectric layer.

52. The method of claim 51, wherein:

said step b) comprises plating shut said first blind via and said second blind via, and

said method includes only a single plating cycle.

53. The method of claim 51, wherein each of said first blind via and said second blind via has an aspect ratio of at least about 1:1.

54. The method of claim 53, wherein each of said interlayer interconnection units has an effective aspect ratio of at least about 2:1.

55. A method for forming a multilayer printed circuit board (PCB), comprising:

a) a step for forming a pseudo three-layer core, wherein said pseudo three-layer core includes:

a first metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer; and

a second metal layer disposed on said second dielectric layer; and

b) a step for forming a plurality of interlayer interconnection units for electrically interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes:

a pair of opposed coaxial blind vias, and

a bridge pad disposed between, and in electrical contact with, said pair of blind vias, wherein said bridge layer comprises a plurality of said bridge pads.

56. A method for forming a pseudo three-layer core for a PCB, comprising:

a) providing a first metal layer;

b) providing a first dielectric layer on said first metal layer;

c) forming a bridge layer on said first dielectric layer, said bridge layer comprising a plurality of bridge pads;

d) providing a second dielectric layer on said bridge layer;

e) providing a second metal layer on said second dielectric layer;

f) forming a first blind via on a first side of each of said plurality of bridge pads, wherein said first blind via extends from said first metal layer through said first dielectric layer; and

g) forming a second blind via on a second side of each of said plurality of bridge pads, wherein said second blind via extends from said second metal layer through said second dielectric layer.

57. The method of claim 56, wherein:

said first dielectric layer comprises a first side and a second side, said first side having said first metal layer disposed thereon, and said second side having a layer of copper foil disposed thereon, and

said step c) comprises etching said layer of copper foil.

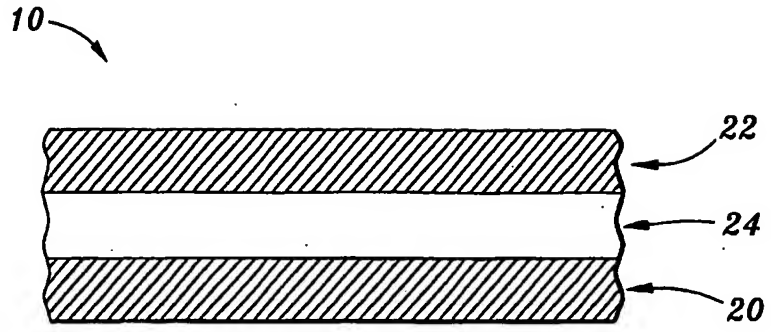

FIG. 1A
(PRIOR ART)

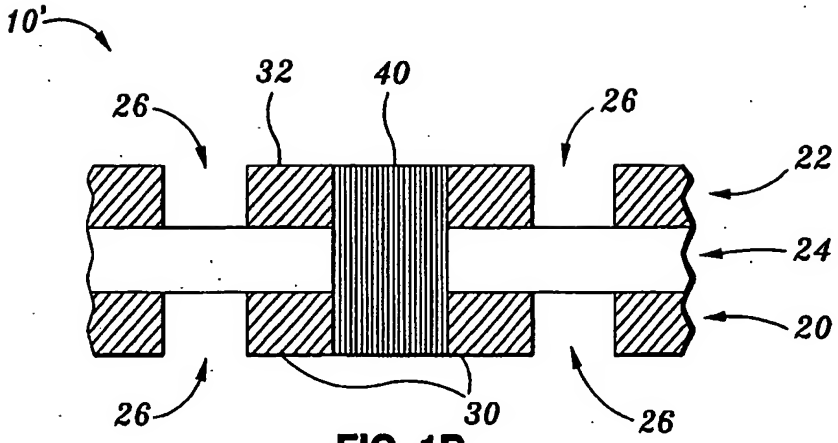

FIG. 1B
(PRIOR ART)

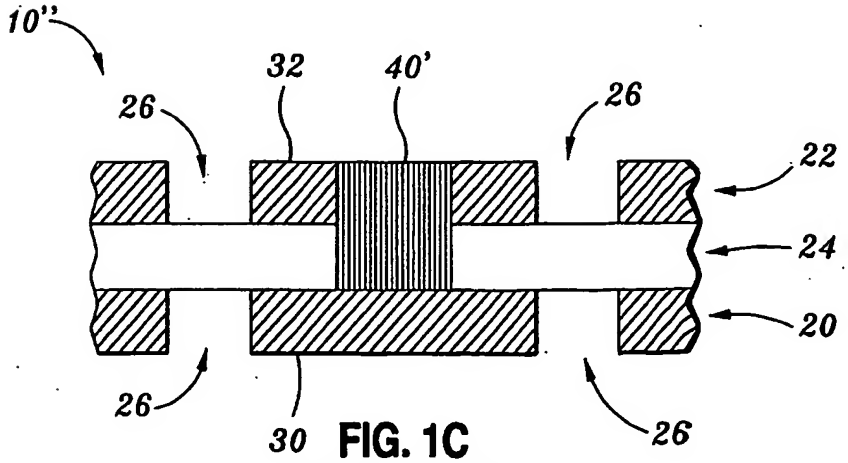

FIG. 1C
(PRIOR ART)

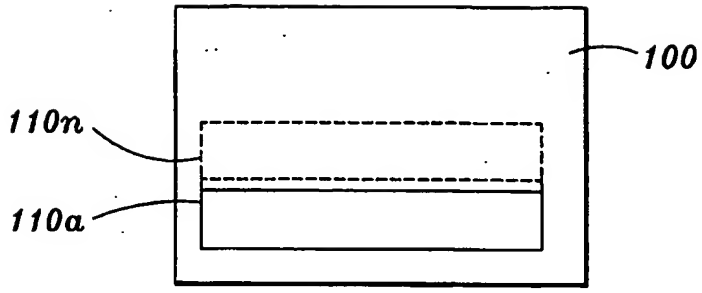
100
110n
110a

FIG. 2

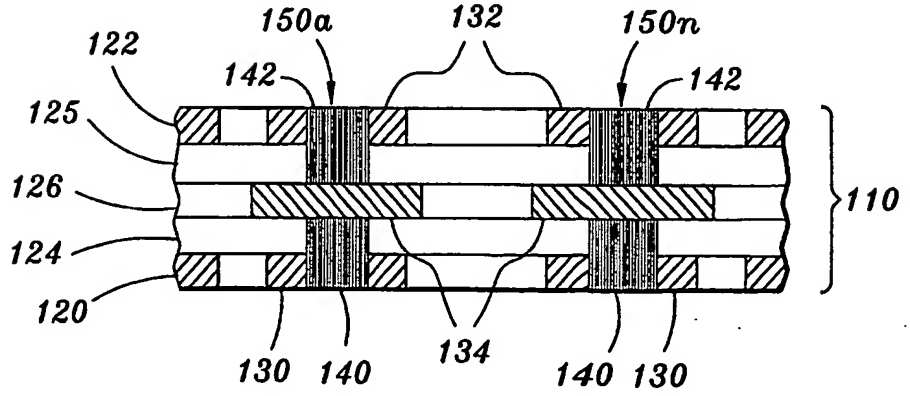
150a
132
150n
122
142
142
125
126
124
120
110
130
140
134
140
130

FIG. 3

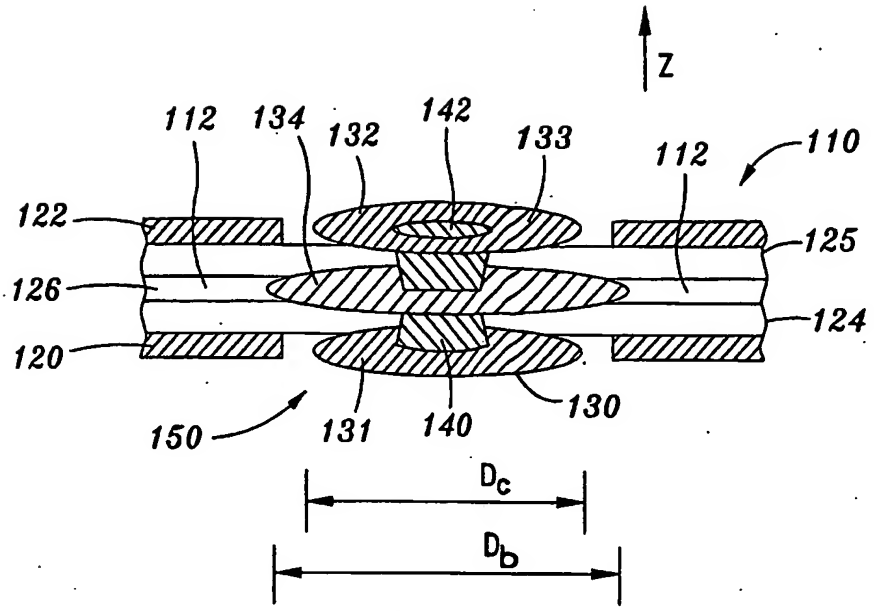
Z
112
134
132
142
133
112
110
122
125
126
124
120
130
150
131
140
D_c
D_b

FIG. 4A

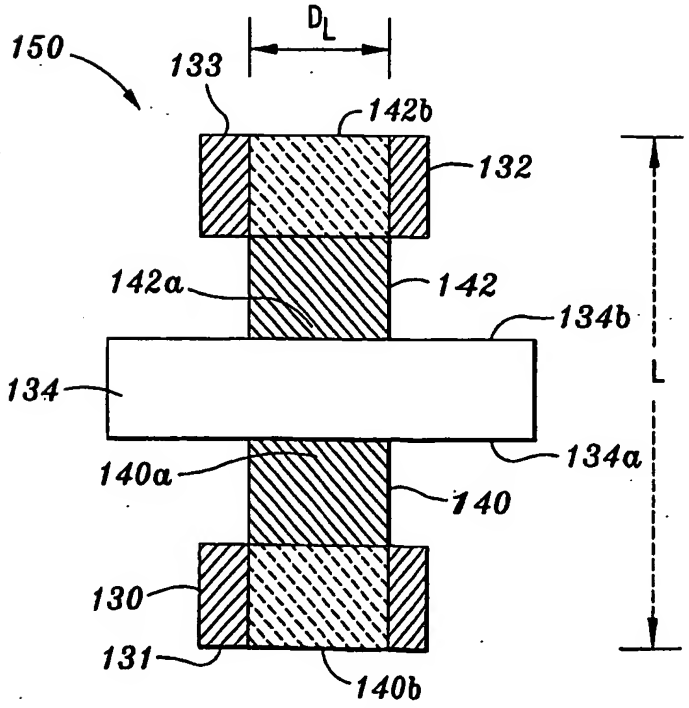
D_L
150
133
142b
132
142a
142
134b
134
L
134a
140a
140
130
131
140b

FIG. 4B

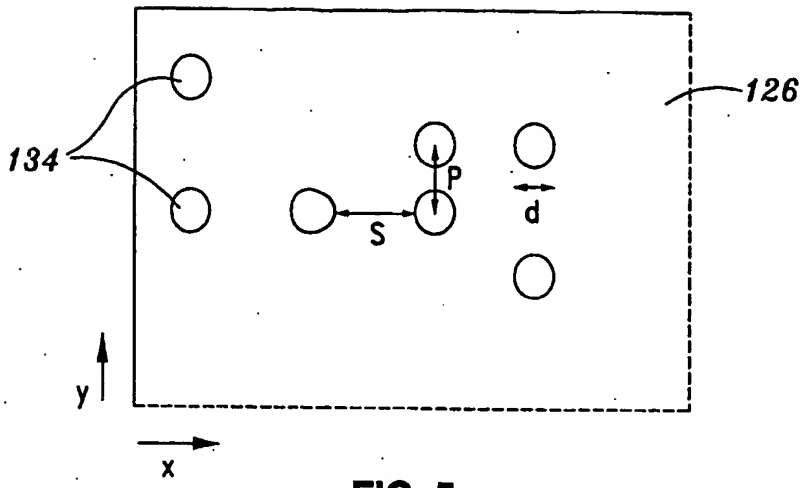

FIG. 5

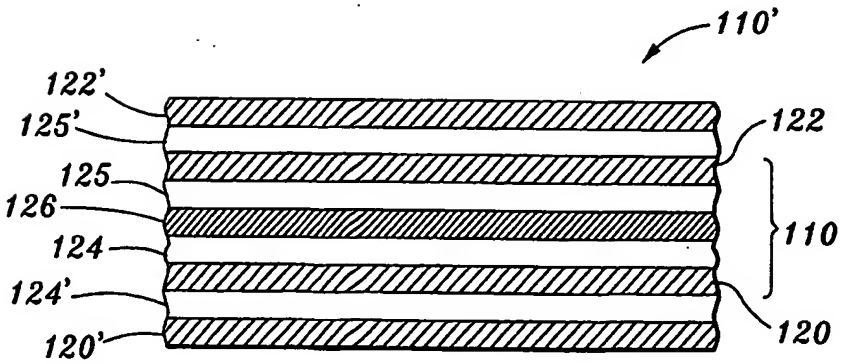

FIG. 6

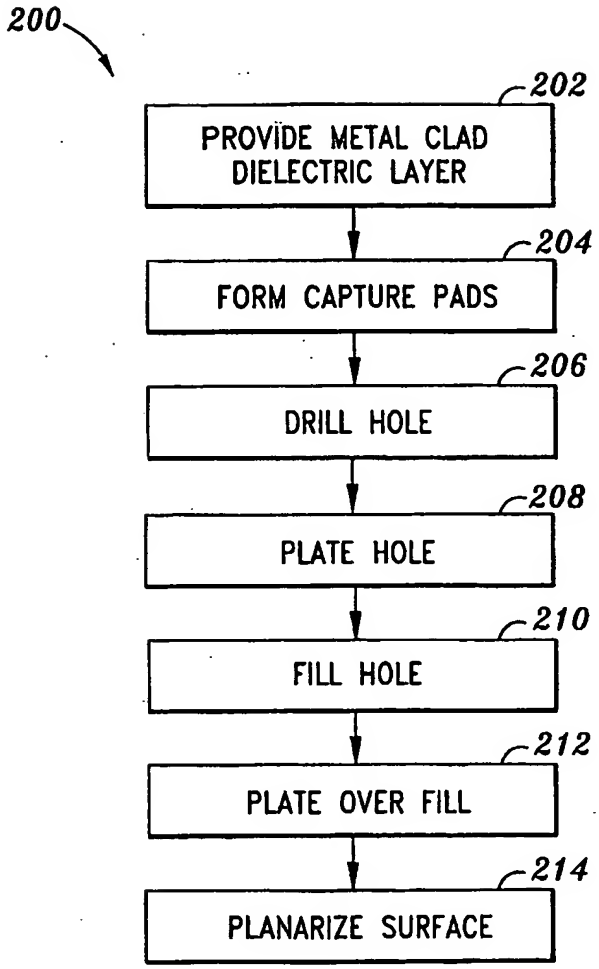

FIG. 7

(PRIOR ART)

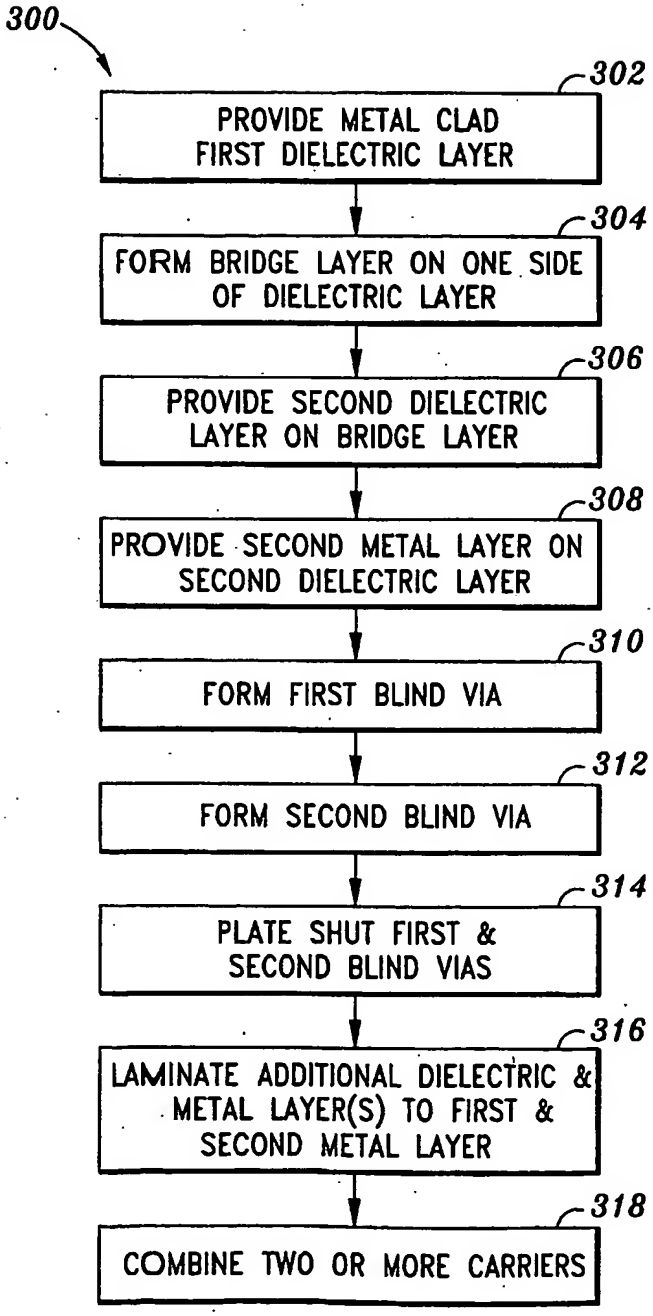
300
302
PROVIDE METAL CLAD FIRST DIELECTRIC LAYER
304
FORM BRIDGE LAYER ON ONE SIDE OF DIELECTRIC LAYER
306
PROVIDE SECOND DIELECTRIC LAYER ON BRIDGE LAYER
308
PROVIDE SECOND METAL LAYER ON SECOND DIELECTRIC LAYER
310
FORM FIRST BLIND VIA
312
FORM SECOND BLIND VIA
314
PLATE SHUT FIRST & SECOND BLIND VIAS
316
LAMINATE ADDITIONAL DIELECTRIC & METAL LAYER(S) TO FIRST & SECOND METAL LAYER
318
COMBINE TWO OR MORE CARRIERS

FIG. 8

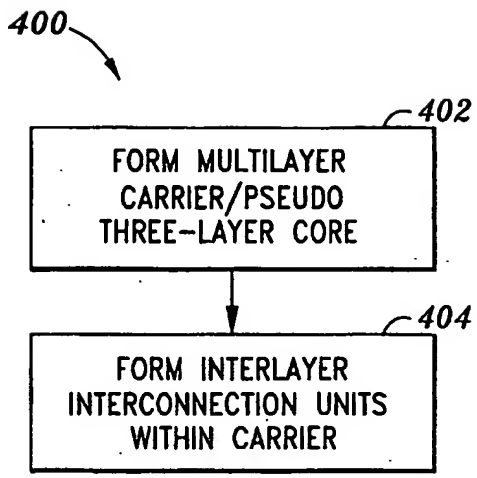
400
402
FORM MULTILAYER CARRIER/PSEUDO THREE-LAYER CORE
404
FORM INTERLAYER INTERCONNECTION UNITS WITHIN CARRIER

FIG. 9

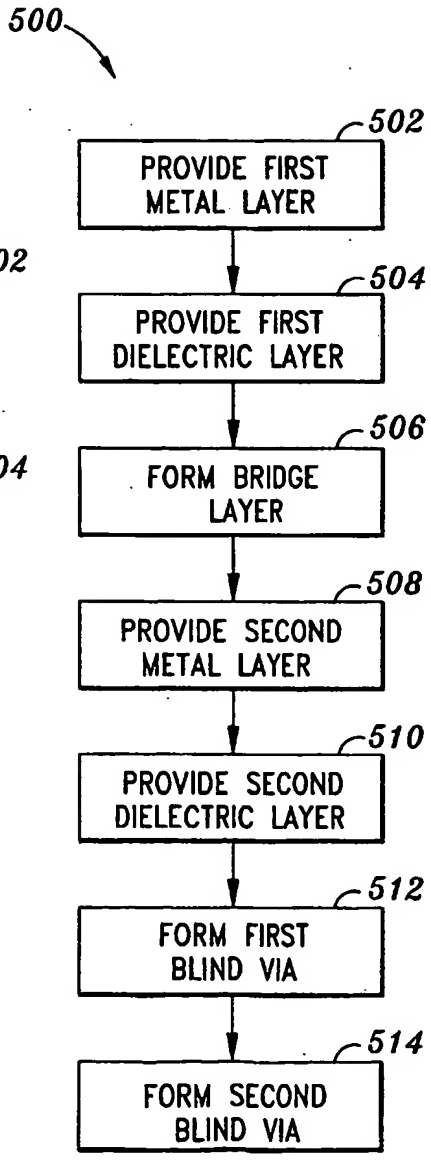
500
502
PROVIDE FIRST METAL LAYER
504
PROVIDE FIRST DIELECTRIC LAYER
506
FORM BRIDGE LAYER
508
PROVIDE SECOND METAL LAYER
510
PROVIDE SECOND DIELECTRIC LAYER
512
FORM FIRST BLIND VIA
514
FORM SECOND BLIND VIA

FIG. 10

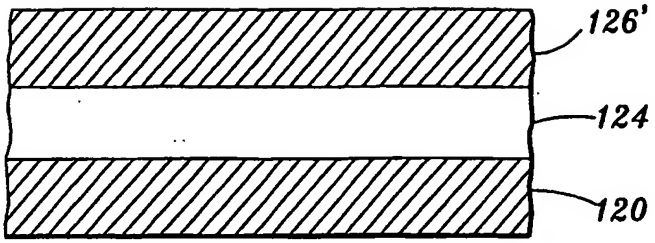

FIG. 11A

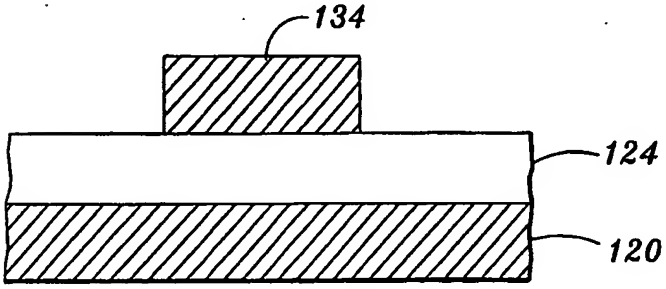

FIG. 11B

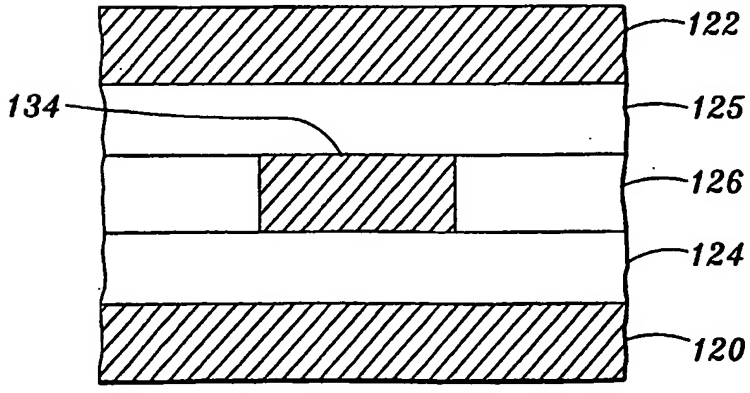

FIG. 11C

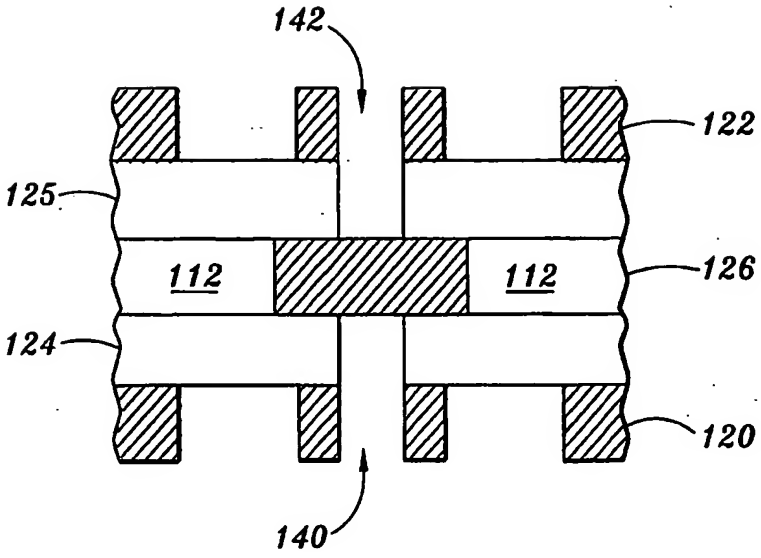

FIG. 11D

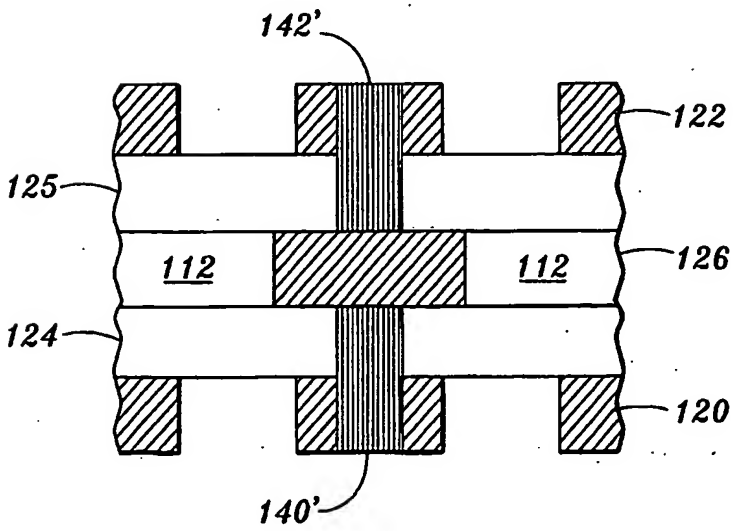

FIG. 11E

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/033012

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05K1/11 H05K3/42 H05K3/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05K H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 2003, no. 05, 12 May 2003 (2003-05-12) & JP 2003 031952 A (MEIKO:KK), 31 January 2003 (2003-01-31) abstract	1-57
P,X	-& EP 1 406 477 A (MEIKO ELECTRONICS CO., LTD) 7 April 2004 (2004-04-07) paragraphs '0023! - '0040!; figures 8-14	1-57
X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 14, 22 December 1999 (1999-12-22) & JP 11 261236 A (ELNA CO LTD), 24 September 1999 (1999-09-24) abstract	1-57

-/—

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 February 2005	25/02/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Batev, P

1

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/033012

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 471 631 A (LEO J. QUINTANA) 7 October 1969 (1969-10-07) the whole document	1-57
X	US 5 347 712 A (YASUDA ET AL) 20 September 1994 (1994-09-20) column 13, line 61 - column 14, line 15; figures 21,22	1-57
X	US 6 548 767 B1 (LEE KYU-WON ET AL) 15 April 2003 (2003-04-15) the whole document	1-57
X	US 5 846 097 A (MARIAN, JR. ET AL) 8 December 1998 (1998-12-08) column 7, line 50 - column 8, line 15; figure 5	1,21,29, 33,40, 51,56

1

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/033012

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2003031952 A	31-01-2003	EP 1406477 A1	07-04-2004
		WO 03009661 A1	30-01-2003
		US 2004136152 A1	15-07-2004
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		US 5913688 A	22-06-1999

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(19) World Intellectual Property Organization
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21 April 2005 (21.04.2005)

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(10) International Publication Number
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10/683,641 9 October 2003 (09.10.2003) US

(71) Applicant *(for all designated States except US)*: QUALCOMM INCORPORATED [US/US]; 5775 Morehouse Drive, San Diego, CA 92121 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: MATTIX, Dwight, W. [US/US]; 1563 Hilltop Drive, El Cajon, CA 92020 (US).

(74) Agents: WADSWORTH, Phillip, R. et al.; 5775 Morehouse Drive, San Diego, CA 92121 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

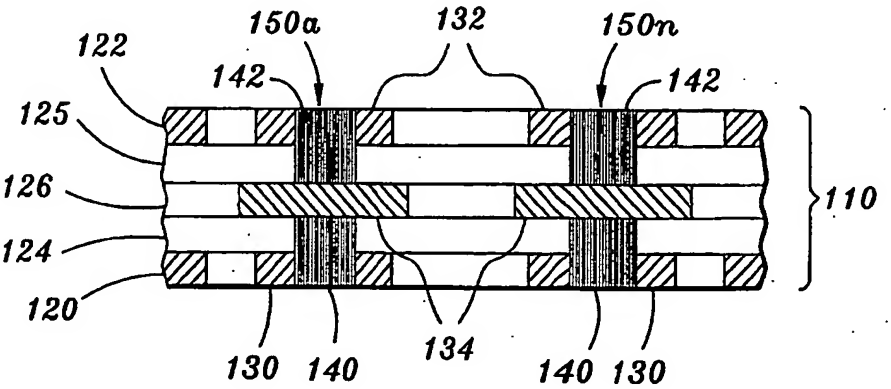
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE,*

[Continued on next page]

(54) Title: TELESCOPING BLIND VIA IN THREE-LAYER CORE



(57) Abstract: A multilayer PCB including at least one carrier, wherein the at least one carrier comprises a pseudo three-layer core (110). Each three-layer core (110) includes a first metal layer (120), a first dielectric layer (124), an internal bridge layer (126), a second dielectric layer (125), and a second metal layer (122). The bridge layer includes a plurality of bridge pads (134). Each carrier includes a plurality of interlayer interconnection units (150a, 150n) for interconnecting the first and second metal layers. Each interlayer interconnection unit comprises a pair of opposed blind vias (140, 142) and a bridge pad (134) disposed between, and in electrical contact with, the pair of blind vias.

WO 2005/036940 A1

BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

TELESCOPING BLIND VIA IN THREE-LAYER CORE

BACKGROUND OF THE INVENTION

[0001] The present invention generally relates to printed circuit boards, and more particularly to multilayer printed circuit boards comprising a three-layer core having a dual blind via interlayer interconnection unit. The present invention also relates to methods for forming a three-layer core of a multilayer printed circuit board.

[0002] The present trend in the design and manufacture of printed circuit boards (PCBs) is towards decreased size, smaller hole or via diameter, and higher interconnection density. High interconnection densities require multilayer PCBs having more than one signal layer with numerous interconnections therebetween.

[0003] Each signal layer of prior art multilayer PCBs typically consists of a patterned conductive metal layer. Adjacent conductive layers are separated by an insulating material or dielectric layer comprising, for example, a polyimide or a resin which may be reinforced with glass fiber. Interconnections between the various conductive layers are provided by holes or vias that extend through the intervening dielectric layer, wherein the vias or holes are plated, filled, and/or plated over with conductive material. Such vias or holes may be through holes, blind vias, or buried vias. Through holes extend to all conductive layers of a multilayer assembly. In contrast, blind vias and buried vias pass through only part of a PCB – blind vias having one end of the via exposed, and buried vias having neither end of the via exposed. Thus, a blind via connects two or more layers of a PCB and starts on an outer layer, but does not pass completely through the PCB. A buried via connects two or more inner layers of a PCB but no outer layer.

[0004] Two-layer cores, which consist of a thin dielectric layer covered with copper foil, form the basic building block of prior art PCBs. Typically, the dielectric layer of a two-layer core is covered with copper foil on both sides. Multilayer PCBs of the prior art may be formed by laminating two or more two-layer cores. After patterning the copper foil of the signal layers, the layers are laminated using heat and pressure. Plated via holes for interlayer connection may be formed by drilling in the z-axis between layers, e.g., by laser drilling, followed by plating the hole. A blind via may be formed by drilling partly through one or more dielectric layers, followed by

plating the hole, or by forming a plated through hole and then laminating an additional layer on one side thereof. A buried via may be formed by forming a blind via and laminating an additional layer on the exposed end of the blind via, or by providing a plated through hole and laminating an additional layer on each side of the plated through hole. Such procedures or processes are well known in the art.

[0005] As noted above, the standard building block of prior art PCBs is a core consisting of a two-layer dielectric carrier. Stacking a μvia on either side of such a carrier requires a solid target pad for laser ablating down to (or building up from with additive technology) the top of the carrier's buried via. This requires creating either a solid copper through via, or a via that is filled and plated over in the carrier. Creation of such vias becomes problematic as via size and dielectric thickness decrease. In order to form a large enough via in the carrier to drill and fill effectively, the minimum producible drill-to-adjacent-feature spacing cannot be maintained. Likewise, filling a through via on a thin carrier has limited producibility due to limitations of via fill and plating processes related to decreased carrier thickness. Also, restrictions on high aspect ratio of the filled hole effectively limit the thickness of the carrier's dielectric layer. However, in certain situations a thicker dielectric layer might be required, e.g., for impedance purposes, or for overall finished dimensions of the PCB. Furthermore, thin dielectric layers, which may be required to maintain a minimum aspect ratio for μvias formed therein, may lack the necessary dimensional stability for processing, e.g., filling a plated hole, which may result in destruction of the carrier.

[0006] In addition, filling a via of the prior art usually requires multiple plating cycles, and consequently may result in unacceptably thick total surface copper for etching fine features on a signal layer. Consequently, a significant portion of the total surface copper may have to be removed by mechanical means during processing according to the prior art.

[0007] Figure 1A is a cross-sectional view of a copper clad dielectric layer 10 for processing into a conventional two-layer carrier for a PCB, according to the prior art. Copper clad dielectric layer 10 includes a first copper layer 20, a second copper layer 22, and a dielectric layer 24 disposed between first and second copper layers 20, 22. Dielectric layer 24 may comprise a dielectric material, such as a glass fiber reinforced resin, or a polyimide, and the like.

[0008] Figure 1B is a cross-sectional view of a conventional carrier 10' for a

PCB in the form of a two-layer core, according to the prior art. Carrier 10' has two metal layers, namely a first copper layer 20 and a second copper layer 22, as well as a dielectric layer 24 disposed between first and second copper layers 20, 22. Carrier 10' includes a plated through hole 40 which has been filled and plated over. Plated through hole 40 extends from a first pad 30 within first copper layer 20 to a second pad 32 within second copper layer 22. Plated through hole 40 serves as a conducting interconnection between first and second copper layers 20, 22. Such plated through holes are well known in the art. Regions of the prior art two-layer core that lack first and second copper layers 20, 22, e.g., due to etching thereof, are represented by reference numeral 26.

[0009] Figure 1C is a cross-sectional view of a conventional carrier 10'' for a PCB in the form of a two-layer core, also according to the prior art. Carrier 10'' includes a dielectric layer 24 disposed between first and second copper layers 20, 22, essentially as described for Figure 1B. Figure 1C shows a blind via 40' which has been filled and plated over. Blind via 40' extends from a first pad 30 within first copper layer 20 to a second pad 32 within second copper layer 22. Blind via 40' serves as a conducting interconnection between different layers of a multilayer PCB, e.g., between first and second copper layers 20, 22. Such blind vias are well known in the art. Regions of prior art carrier 10'' that lack first and second copper layers 20, 22, e.g., due to etching thereof, are represented by reference numeral 26.

[0010] As noted hereinabove, conventional two-layer cores of the prior art have a number of drawbacks and disadvantages. As an example, as hole size (e.g., via diameter) diminishes to accommodate higher interconnect densities, dielectric thickness must also decrease in order to maintain a certain minimum aspect ratio for the hole, since holes having aspect ratios below the producible minimum cannot be filled efficiently or reliably. Restrictions on dielectric thickness, in turn, are associated with a number of other disadvantages. However, dielectrics below a certain thickness cannot be processed reliably, leading to destruction of many incipient cores and poor processing efficiency. For example, increased dielectric thickness may be required for impedance purposes. Furthermore, a PCB having a relatively large overall dielectric thickness may offer advantages for providing connections thereto. In addition, increased overall dielectric thickness may allow for production of a PCB having a greater overall finished thickness, for example, to fit within a particular housing of an

instrument, device, or appliance.

[0011] As can be seen, there is a need for a multilayer PCB having an interlayer interconnection unit, the formation of which requires only a single plating cycle. The use of only a single plating cycle can result in decreased thickness of total surface copper, thereby facilitating formation of fine features without the need for mechanical reduction of the surface copper layer. There is also a need for a dual via interlayer interconnection unit for a multilayer PCB, wherein the interconnection unit allows an overall increased aspect ratio, as compared with prior art plated through holes and vias. There is a further need for a PCB core or subassembly wherein the total thickness of the dielectric, at minimum hole and pad diameter, can be increased when greater dielectric thickness is required, for example, for impedance purposes or for overall finished thickness.

SUMMARY OF THE INVENTION

[0012] In one aspect of the present invention, an interlayer interconnection unit for a multi-layer printed circuit board (PCB) comprises an interstitial bridge pad having a first side and a second side, wherein the interstitial bridge pad is disposed between a first dielectric layer and a second dielectric layer; a first blind via disposed on the first side of the interstitial bridge pad, wherein the first blind via extends through the first dielectric layer; and a second blind via disposed on the second side of the interstitial bridge pad, wherein the second blind via extends through the second dielectric layer.

[0013] In another aspect of the present invention, an interlayer interconnection unit for a multi-layer PCB comprises a first capture pad having a first annular ring; a first via having a first via inner end and a first via outer end, with the first via outer end in contact with the first capture pad and encircled by the first annular ring; an interstitial bridge pad having a first side and a second side, with the first via inner end in contact with the first side of the interstitial bridge pad; a second via having a second via inner end and a second via outer end, with the second via inner end in contact with the second side of the interstitial bridge pad; and a second capture pad having a second annular ring, with the second via outer end in contact with the second capture pad and encircled by the second annular ring.

[0014] In yet another aspect of the present invention, a dual blind via interconnection unit for a multilayer PCB comprises a pair of opposed coaxial blind vias; and a bridge pad disposed between the pair of blind vias, wherein each of the pair of blind vias is in contact with the bridge pad.

[0015] In still another aspect of the present invention, a carrier for a multi-layer PCB comprises a pseudo three-layer core. The pseudo three-layer core includes a first metal layer, a first dielectric layer disposed on the first metal layer, a bridge layer disposed on the first dielectric layer, a second dielectric layer disposed on the bridge layer, and a second metal layer disposed on the second dielectric layer. The bridge layer comprises a plurality of spaced apart interstitial bridge pads, and each of the plurality of interstitial bridge pads is adapted for providing an interlayer interconnection between the first metal layer and the second metal layer.

[0016] In a further aspect of the present invention, a pseudo three-layer core for a PCB may comprise a plurality of interlayer interconnection units, wherein each of the interlayer interconnection units extends from a first metal layer to a second metal layer; a first dielectric layer disposed on the first metal layer; a bridge layer disposed on the first dielectric layer; and a second dielectric layer disposed on the bridge layer, wherein the second metal layer is disposed on the second dielectric layer. Each of the interlayer interconnection units may comprise an interstitial bridge pad located within the bridge layer, a first blind via extending from the first metal layer to a first side of the interstitial bridge pad, and a second blind via extending from the second metal layer to a second side of the interstitial bridge pad.

[0017] In yet a further aspect of the present invention, a multi-layer PCB comprises a first signal layer; a second signal layer; a bridge layer disposed between the first signal layer and the second signal layer; and a plurality of interlayer interconnection units. Each of the interlayer interconnection units may be adapted for connecting the first signal layer with the second signal layer through the bridge layer.

[0018] In still a further aspect of the present invention, a multi-layer PCB comprises at least one pseudo three-layer core. Each pseudo three-layer core may include a first metal layer, a first dielectric layer disposed on the first metal layer, a bridge layer disposed on the first dielectric layer, a second dielectric layer disposed on the bridge layer, a second metal layer disposed on the second dielectric layer, and a

plurality of interlayer interconnection units. Each of the interlayer interconnection units may comprise an interstitial bridge pad having a first side and a second side, a first blind via disposed on the first side of the interstitial bridge pad, and a second blind via disposed on the second side of the interstitial bridge pad.

[0019] In an additional aspect of the present invention, a multilayer PCB may comprise a means for carrying a plurality of signal layers; and a plurality of means for interconnecting at least two of the signal layers, wherein the carrying means comprises a pseudo three-layer core, wherein the pseudo three-layer core includes an internal bridge layer, wherein the bridge layer comprises a plurality of interstitial bridge pads, and wherein each of the interconnecting means comprises a pair of opposed blind vias disposed on either side of each of the interstitial bridge pads.

[0020] In yet an additional aspect of the present invention, a method for forming a multilayer PCB comprises providing a metal clad first dielectric layer having a first metal clad side and a second metal clad side; forming a bridge layer from the second metal clad side, wherein the bridge layer comprises a plurality of bridge pads, and wherein the first metal clad side comprises a first metal layer; providing a second dielectric layer on the bridge layer, wherein the second dielectric layer has a second metal layer disposed thereon; forming a plurality of first blind vias through the first dielectric layer, with the plurality of first blind vias extending from the first metal layer to a first side of each of the plurality of bridge pads; and forming a plurality of second blind vias through the second dielectric layer, with the plurality of second blind vias extending from the second metal layer to a second side of each of the plurality of bridge pads.

[0021] In still a further aspect of the present invention, a method for forming a multilayer PCB comprises forming a pseudo three-layer core, wherein the pseudo three-layer core includes a first metal layer, a first dielectric layer disposed on the first metal layer, a bridge layer disposed on the first dielectric layer, a second dielectric layer disposed on the bridge layer, and a second metal layer disposed on the second dielectric layer, wherein the bridge layer comprises a plurality of spaced apart interstitial bridge pads. The method further comprises forming a plurality of interlayer interconnection units for interconnecting the first metal layer and the second metal layer, wherein each of the interlayer interconnection units includes a first blind via disposed on a first side of one of the plurality of interstitial bridge pads, wherein the first blind via extends from

the first metal layer through the first dielectric layer; and a second blind via disposed on a second side of one of the plurality of interstitial bridge pads, wherein the second blind via extends from the second metal layer through the second dielectric layer.

[0022] In yet an additional aspect of the present invention, a method for forming a multilayer PCB comprises a step for forming a pseudo three-layer core, wherein the pseudo three-layer core includes a first metal layer, a first dielectric layer disposed on the first metal layer, a bridge layer disposed on the first dielectric layer, a second dielectric layer disposed on the bridge layer, and a second metal layer disposed on the second dielectric layer, wherein the bridge layer comprises a plurality of bridge pads. The method further comprises a step for forming a plurality of interlayer interconnection units for interconnecting the first metal layer and the second metal layer, wherein each of the interlayer interconnection units includes a first blind via disposed on a first side of one of the plurality of interstitial bridge pads, wherein the first blind via extends from the first metal layer through the first dielectric layer, and a second blind via disposed on a second side of one of the plurality of interstitial bridge pads, wherein the second blind via extends from the second metal layer through the second dielectric layer.

[0023] In still another aspect of the present invention, a method for forming a pseudo three-layer core for a PCB comprises providing a first metal layer; providing a first dielectric layer on the first metal layer; forming a bridge layer on the first dielectric layer, wherein the bridge layer comprises a plurality of bridge pads; providing a second dielectric layer on the bridge layer; providing a second metal layer on the second dielectric layer; forming a first blind via on a first side of each of the plurality of bridge pads, wherein the first blind via extends from the first metal layer through the first dielectric layer; and forming a second blind via on a second side of each of the plurality of bridge pads, wherein the second blind via extends from the second metal layer through the second dielectric layer.

[0024] These and other features, aspects, and advantages of the present invention will become better understood with reference to the following drawings, description, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Figure 1A is a cross-sectional view of a copper clad dielectric layer for processing into a conventional two-layer carrier for a printed circuit board (PCB), according to the prior art;

[0026] Figure 1B is a cross-sectional view of a conventional carrier for a PCB in the form of a two-layer core having a plated through hole therein, also according to the prior art;

[0027] Figure 1C is a cross-sectional view of a conventional carrier for a PCB in the form of a two-layer core having a blind via therein, also according to the prior art;

[0028] Figure 2 is a block diagram schematically representing a multilayer PCB having at least one carrier comprising a pseudo three-layer core, according to one embodiment of the present invention;

[0029] Figure 3 schematically represents a plurality of interlayer interconnection units within a portion of a pseudo three-layer core, as seen in sectional view, according to one embodiment of the present invention;

[0030] Figure 4A is a perspective view of an interlayer interconnection unit within a pseudo three-layer core, according to one embodiment of the present invention;

[0031] Figure 4B is a side view of the interlayer interconnection unit of Figure 4A, according to the present invention;

[0032] Figure 5 is a plan view of a portion of a bridge layer of a carrier for a multilayer PCB, according to one embodiment of the present invention;

[0033] Figure 6 schematically represents a carrier for a multilayer PCB having additional conductive layers on a pseudo three-layer core, according to one embodiment of the present invention;

[0034] Figure 7 schematically represents a series of steps involved in a method for making a conventional carrier for a multilayer PCB, according to the prior art;

[0035] Figure 8 schematically represents a series of steps involved in a method for making a multilayer PCB, according to another embodiment of the present invention;

[0036] Figure 9 schematically represents a series of steps involved in a method for making a multilayer PCB, according to yet another embodiment of the present invention;

[0037] Figure 10 schematically represents a series of steps involved in a method

for making a carrier for a multilayer PCB, according to a further embodiment of the present invention; and

[0038] Figures 11A-E illustrate stages in a process for forming an interlayer interconnection unit for a multilayer PCB, according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0039] The following detailed description is of the best currently contemplated modes of carrying out the invention. The description is not to be taken in a limiting sense, but is made merely for the purpose of illustrating the general principles of the invention, since the scope of the invention is best defined by the appended claims.

[0040] Generally, the present invention provides a carrier for a multilayer printed circuit board (PCB) or printed wiring board, wherein the carrier may include a novel interlayer interconnection unit for interconnecting a plurality of conductive layers of the multilayer PCB. A basic carrier, sub-assembly, or building block according to one embodiment of the invention may comprise a pseudo three-layer core. Each pseudo three-layer core may comprise two signal layers for a multilayer PCB, wherein the two signal layers are interconnected through an interconnection unit comprising an internal bridge layer disposed between the two signal layers.

[0041] A pseudo three-layer core of the present invention may have additional layers added thereto. For example, a multilayer PCB of the invention may comprise a single pseudo three-layer core, and up to six (6) or more conductive layers. A plurality of carriers may be combined, e.g., laminated together, to form a multilayer PCB having up to about 28 or more signal layers. Multilayer PCBs find almost universal applications in electrical or electronic devices, instruments, and appliances.

[0042] In contrast to a conventional two-layer core of the prior art, for example, as described hereinabove with reference to Figures 1B-C, in one embodiment the present invention provides a carrier having two dielectric layers, a bridge layer disposed between the two dielectric layers, and a pair of external conductive layers. As compared with carriers of the present invention, prior art carriers, i.e., two-layer cores of prior art multilayer PCBs, have only a single dielectric layer and lack a bridge layer. As compared with prior art multilayer PCBs which have a carrier comprising a two-layer core in which a single dielectric layer is disposed between two conductive layers,

multilayer PCBs of the present invention have a carrier comprising a three-layer core, or pseudo three-layer core, including a pseudo metal layer or bridge layer disposed between two dielectric layers.

[0043] The bridge layer of carriers of the present invention may be referred to as a pseudo metal layer in that the bridge layer is not a metal layer of the type encountered in prior art carriers, for example, due to the lack of electrical connectivity within the bridge layer between the metal bridge pads that constitute the bridge layer. Due to the presence of the internal pseudo metal (bridge) layer in carriers of the present invention, the basic carrier of the invention, which may comprise the bridge layer, the two dielectric layers, and the pair of external conductive layers, may be referred to as a pseudo three-layer core. The pair of outer conductive layers may be interconnected by a plurality of interlayer interconnection units, wherein each interconnection unit may comprise an interstitial bridge pad located within the bridge layer, and a pair of coaxial, opposed blind vias disposed on either side of the interstitial bridge pad.

[0044] In some embodiments of the present invention, a pseudo three-layer core of the invention may itself constitute a multilayer PCB. In other embodiments of the invention, additional dielectric layers and additional conductive (e.g., signal) layers may be sequentially laminated to the pseudo three-layer core. Furthermore, two or more pseudo three-layer cores of the present invention, with or without additional dielectric and conductive layers, may be laminated to each other to form multilayer PCBs having up to 28 or more signal layers.

[0045] Figure 2 is a block diagram schematically representing a multilayer PCB 100, according to one embodiment of the present invention. Multilayer PCB 100 may include a first carrier or core 110a. In some embodiments, multilayer PCB 100 may further include one or more additional carriers 110n. The one or more additional carriers 110n may be laminated to first carrier 110a. Each of first carrier 110a and additional carrier(s) 110n may comprise a pseudo three-layer core of the present invention. Each pseudo three-layer core may comprise two signal layers. Such a pseudo three-layer core is described fully hereinbelow, for example, with respect to Figures 4A-B. In some embodiments, one or more of first carrier 110a and additional carriers 110n may further comprise one or more additional signal layers 120', 122' (Figure 6).

[0046] Figure 3 is a sectional view showing a plurality of interlayer interconnection units within a portion of a pseudo three-layer core 110, according to an embodiment of the present invention. Pseudo three-layer core 110 may include a first interlayer interconnection unit 150a, and an n^{th} interlayer interconnection unit 150n. Pseudo three-layer core 110 may include a first metal layer 120, a first dielectric layer 124 disposed on first metal layer 120, a bridge layer 126 disposed on first dielectric layer 124, a second dielectric layer 125 disposed on bridge layer 126, and a second metal layer 122 disposed on second dielectric layer 125. Each of interlayer interconnection units 150a and 150n extend from first metal layer 120, through bridge layer 126, to second metal layer 122. For the purpose of clarity, only two interconnection units 150a, 150n are shown in Figure 3. In practice, pseudo three-layer core 110 may include any number of interlayer interconnection units. Typically, interlayer interconnection units 150a, 150n may be present only at locations, with respect to the x and y dimensions of a PCB, at which it is desired to interconnect first metal layer 120 to second metal layer 122. Locations at which interlayer interconnection units 150a, 150n may be present correspond to the locations of bridge pads 134. Such locations of bridge pads 134 are schematically represented in Figure 5. The x and y dimensions are shown in Figure 5 by the arrows labeled "x" and "y" respectively. Interlayer interconnection units of the present invention are further described hereinbelow, e.g., with reference to Figures 4A-B.

[0047] Figure 4A shows an interlayer interconnection unit 150 within a three-layer core 110, with interlayer interconnection unit 150 shown in perspective view, according to one embodiment of the present invention. Three-layer core 110 may include an internal bridge layer 126 disposed between first dielectric layer 124 and second dielectric layer 125. Three-layer core 110 may further include first and second metal layers 120, 122, respectively, as described hereinabove.

[0048] Bridge layer 126 may comprise a plurality of spaced apart interstitial bridge pads 134. Each bridge pad 134 may comprise an essentially disc-shaped conductive element, e.g., a copper disc. Each bridge pad 134 may lack electrical connection to other bridge pads 134 within bridge layer 126. Interlayer interconnection unit 150 may include one bridge pad 134 located within bridge layer 126 (Figure 5).

That is to say, each bridge pad 134 may be a component of an interlayer interconnection unit 150.

[0049] Interlayer interconnection unit 150 may further include a first capture pad 130 within first metal layer 120, and a second capture pad 132 within second metal layer 122. First capture pad 130 and second capture pad 132 may each comprise a conductive (e.g., copper) element, which may be formed by the selective removal, e.g., by etching, of first metal layer 120 and second metal layer 122, respectively. It is apparent from Figure 4A that bridge pad 134 may have a diameter, D_b that is greater than a diameter, D_c of first and second capture pads 130, 132. First Interlayer interconnection unit 150 may still further include a first blind via 140 and a second blind via 142. Each of first blind via 140 and second blind via 142 may be formed by a process such as laser drilling, plasma drilling, or photo-definition (photo-defining). Although Figure 4A shows a gap 112 within bridge layer 126 on either side of bridge pad 134, during lamination first and second dielectric layers 124, 125 may fuse together such that bridge pad 134 may be encapsulated within first and second dielectric layers 124, 125.

[0050] During formation of interlayer interconnection unit 150, a first annular ring 131 may be formed within first metal layer 120. As an example, first annular ring 131 may comprise an annular, outer portion of first capture pad 130. Similarly, during formation of interlayer interconnection unit 150, a second annular ring 133 may be defined within second metal layer 122. As an example, second annular ring 133 may comprise an annular, outer portion of second capture pad 132. Each of first annular ring 131 and second annular ring 133 may comprise an annular conductive (e.g., copper) element.

[0051] After forming first and second blind vias 140, 142, respectively, first and second blind vias 140, 142 may be plated shut. In some embodiments, first and second blind vias 140, 142 may be plated shut using a μfill process, such as the MicroFill™ VF process of the Shipley Company, LLC (Marlborough, MA). Briefly, MicroFill™ VF is a direct current electrolytic copper plating process for filling blind vias, including μvias. (See, for example, *MicroFill™ VF, Electrolytic Copper Plating Technology for Filling Blind Microvias in HDI/Build-up Printed Wiring Boards*, Ref. No. PM02N006, Rev. No. 0, Copyright, 2002, Shipley Company, LLC (Marlborough, MA); and *MicroFill VF Process Manual*, Ref. No. PM03N002, Rev. No. 0, February, 2003, Shipley Company,

LLC (Marlborough, MA), both of which are incorporated by reference herein).

[0052] Figure 4B is a side view of the interlayer interconnection unit of Figure 4A, according to the present invention. First and second dielectric layers 124, 125 are omitted from Figure 4B for the sake of clarity. As may be seen in Figures 4A-B, bridge pad 134 may include a first side 134a and a second side 134b. First blind via 140 may include a first via inner end 140a and a first via outer end 140b. Inner end 140a may be in electrical contact with bridge pad first side 134a, while outer end 140b may be in electrical contact with first capture pad 130 and encircled by first annular ring 131. Second blind via 142 may include a second via inner end 142a and a second via outer end 142b. Inner end 142a may be in electrical contact with bridge pad second side 134b, while outer end 142b may be in electrical contact with second capture pad 132 and encircled by second annular ring 133. First and second annular rings 131, 133, may be considered to be the remaining annular portion of first and second capture pads 130, 132, respectively, after formation of a hole therethrough. Thus, interlayer interconnection unit 150 may extend from first capture pad 130, through first blind via 140, bridge pad 134, second blind via 142, and thence to second capture pad 132.

[0053] Again with reference to Figures 4A-B, each of first and second blind vias 140, 142, respectively, may have an aspect ratio of about 1:1, and usually at least about 1:1. Because first and second blind vias 140, 142 are aligned in the z dimension, or coaxial with each other, interlayer interconnection unit 150 may have an effective aspect ratio of about 2:1, and often greater than 2:1. Thus, interlayer interconnection unit 150 of the instant invention allows for a greater than two fold (2X) increase in effective aspect ratio for interconnecting adjacent conductive layers of multilayer PCBs, as compared with the prior art. At the same time, because pseudo three-layer core 110 of the instant invention has two dielectric layers and two signal layers (as compared with only one dielectric layer in prior art two-layer cores) the total dielectric thickness (i.e., the combined thickness of first and second dielectric layers 124, 125) per signal layer (e.g., the mean thickness of first metal layer 120 and second metal layer 122) may be increased by about two fold in carriers of the present invention as compared with a prior art two-layer core. This increase in total dielectric thickness per signal layer is achieved without increasing the aspect ratio of each blind via, i.e., of first and second blind vias 140, 142. The effective aspect ratio of interlayer interconnection unit 150, as referred to herein, is the ratio of the length, L (Figure 4B) (i.e., the z dimension) of interlayer

interconnection unit 150 to the diameter, D_v (Figure 4B) of first and second blind vias 140, 142. The z axis is indicated in Figure 4A by the vertical arrow labeled "z".

[0054] Figure 5 is a plan view of a portion of a bridge layer 126 of a carrier for a multilayer PCB of the present invention. Bridge layer 126 may include a plurality of interstitial bridge pads 134. Each interstitial bridge pad 134 may comprise a metal, such as copper. The plurality of interstitial bridge pads 134 may be conveniently formed by etching one side of a copper clad dielectric layer 124 (e.g., Figures 11A-B).

[0055] Interstitial bridge pads 134 may be spaced apart from each other by a distance, S in the range of from about 0.7 to 4 mils, with a center-to-center pitch, P in the range of from about 15 to 25 mils. Each interstitial bridge pad 134 may have a diameter, d in the range of from about 12 to 20 mils, usually in the range of from about 14 to 17 mils, and often in the range of from about 15 to 16 mils. Interstitial bridge pads 134 typically lack electrical connectivity, within bridge layer 126, to other bridge pads 134, or to any other conductive element (e.g., a trace or a component) of bridge layer 126. That is to say, bridge layer 126 may consist of a plurality of spaced apart bridge pads 134, with no electrical connections therebetween within bridge layer 126.

[0056] Figure 6 schematically represents a carrier 110' for a multilayer PCB, according to one embodiment of the present invention. Carrier 110' may include a pseudo three-layer core 110. As shown, carrier 110' may further include a first additional dielectric layer 124' and a first additional conductive layer 120' laminated thereto. Carrier 110' may still further include a second additional dielectric layer 125' and a second additional conductive layer 122' laminated thereto. In other embodiments of the invention (not shown in Figure 6), carrier 110' may have fewer or more additional dielectric and conductive layers than those shown in Figure 6 laminated to pseudo three-layer core 110.

[0057] As described hereinabove, pseudo three-layer core 110 may itself comprise two signal layers 120, 122. By adding additional conductive layers, e.g., layers 120', 122' to pseudo three-layer core 110, each carrier 110' may comprise from three to six or more conductive layers (only four conductive layers 120, 122, 120', and 122' are shown in Figure 6). Each of layers 120, 122, 120', and 122', or of any other additional conductive layers (not shown in Figure 6) of a carrier or multilayer PCB 100 may comprise a signal layer; or one or more conductive layers (e.g., layers 120, 122, 120', and 122', or other additional conductive layers) of a carrier or multilayer PCB 100

may comprise a plane or ground layer, as is well known in the art. Two or more carriers 110' may be combined (laminated) together (Figure 2) to form a multilayer PCB having from four to 28 or more conductive layers (see, e.g., Figure 6).

[0058] Figure 7 schematically represents a series of steps (202-214) involved in a method 200 for making a conventional carrier for a multilayer PCB, according to the prior art. Step 202 involves providing a metal clad dielectric layer, such as a layer of dielectric material having a layer of copper foil on each side. Due to production limitations associated with filling μvias of a defined diameter and aspect ratio in a thin dielectric layer, the minimum thickness of the dielectric layer in prior art PCBs is typically about 4 mils.

[0059] Step 204 involves forming pads (capture pads and target pads) on the copper layers by etching the copper foil. The formation of such pads is well known in the art. Due to the industry trend towards high-density interconnections, the diameter of current state of the art capture pads and target pads is typically limited to around 10 mils. In prior art processing, there may be difficulties in aligning the drill to pads of this size. In comparison, bridge pads 134 of the invention may have diameters, d up to about 20 mils or more. The larger diameter, d f bridge pads 134 of the invention is possible because the pseudo metal layer (or bridge layer) 126 of carriers of the invention may lack traces, components, or other conductive features. The larger diameter of bridge pads 134 of the invention offer the advantage of facilitating drill registration during via formation.

[0060] Step 206 involves drilling a hole though one or both of the copper layers and the dielectric layer, to form a blind via or a through hole. Step 208 involves plating the hole. Thereafter, step 208, which entails a first plating cycle of the prior art process, adds to the overall thickness of the surface copper. Step 210 involves filling the hole with electrically conductive material, such as a high solids epoxy. Filling the hole in this manner becomes impracticable for presently used dielectric thickness, hole diameter, and aspect ratio. Step 212 involves plating over the fill, in a second plating cycle, to provide a contiguous metal layer over the filled hole. Thus, step 212 further adds to the surface copper thickness.

[0061] Excessive thickness of surface copper may prevent etching of fine features. For example, for a PCB having a 3 mil line and space specification, a surface copper thickness of 1.4 mils or less may be required. Prior art processes that result in

surface copper thickness greater than 1.4 mils may require additional processing steps to remove excess surface copper.

[0062] Step 214 of the prior art process involves planarizing the copper layer(s) in which holes have been drilled, plated, filled, and plated over. Planarizing may be accomplished by mechanical reduction of surface copper, which process may excessively stress the carrier. In situations, where surface copper exceeds the maximum permissible thickness, reduction of surface copper may damage or destroy the carrier or its components, leading to decreased manufacturing efficiency.

[0063] In contrast to the prior art, processes of the invention for making a multilayer PCB may use only one plating cycle. As a result, a total surface copper thickness of about 1 mil or less can be readily achieved. Lower total surface copper thickness decreases the amount of planarizing and mechanical reduction of surface copper, and allows finer line and space resolution.

[0064] Figure 8 schematically represents a series of steps (302-318) which may be involved in a method 300 for making a multilayer PCB, according to one embodiment of the present invention. Step 302 may involve providing a metal clad first dielectric layer, such as a dielectric layer having a first side and a second side, and a layer of copper foil on both the first side and the second side. Step 304 may involve forming a bridge layer on one side of the dielectric layer. The bridge layer may comprise a plurality of spaced apart bridge pads, as described herein (Figures 4A-B, Figure 5). The bridge layer may be formed by etching the copper foil on one side of the dielectric layer. Alternatively, the bridge pads and the bridge layer may be formed by building up from an exposed dielectric layer using an additive technology. The bridge layer formed during step 302 may be referred to as a pseudo metal layer.

[0065] Step 306 may involve providing a second dielectric layer disposed on the bridge layer. Step 308 may involve providing a second metal layer laminated to the second dielectric layer. Steps 306 and 308 may be combined into a single process in which a dielectric layer, which has been clad with the second metal layer, may be disposed on the bridge layer.

[0066] Step 310 may involve forming a first blind via, wherein the first blind via extends from the first metal layer, through the first dielectric layer, and to a first side of a bridge pad within the bridge layer. Step 312 may involve forming a second blind via

from the second metal layer, through the second dielectric layer, and to a second side of the bridge pad within the bridge layer. Each of the first blind via and the second blind via 142 may be formed by a process such as laser drilling, plasma drilling, or photo-defining. Typically, the first blind via may emanate from a first capture pad of the first metal layer, and the second blind via may emanate from a second capture pad of the second metal layer. The first and second capture pads may be formed by etching the first and second metal layers, respectively.

[0067] Step 314 may involve plating shut the first and second blind vias, such that an interlayer interconnection unit may be formed within a multilayer carrier, wherein the interlayer interconnection unit may include a bridge pad disposed between the first and second blind vias (Figure 4A). The first and second blind vias may be opposed to each other in the z dimension and coaxial with the bridge pad. The first and second blind vias may be plated shut in a single plating cycle using a μfill process, such as the MicroFill™ VF process of the Shipley Company, LLC (Marlborough, MA), as referred to hereinabove.

[0068] Optional step 316 may involve laminating one or more additional dielectric layers, and one or more additional metal layers, to the first and second metal layers of the basic carrier or pseudo three-layer core formed by steps 302-314. In this way, a carrier having up to six or more signal layers may be formed. Optional step 318 can involve laminating together two or more carriers formed by steps 302-314, or by steps 302-316, to provide a multilayer PCB having from 4 to 28 or more signal layers.

[0069] Figure 9 schematically represents a series of steps (402-404) involved in a method 400 for making a multilayer PCB, according to another embodiment of the present invention. Step 402 may involve forming a multilayer carrier or a pseudo three-layer core. A pseudo three-layer core formed according to step 402 may include two signal layers. In some embodiments, the multilayer carrier or pseudo three-layer core may be considered to be a sub-assembly for the multilayer PCB. For example, additional signal layers may be laminated to the pseudo three-layer core; or two or more pseudo three-layer cores may be laminated together to form a multilayer PCB having at least 4 signal layers. Step 404 may involve forming a plurality of interlayer interconnection units within the carrier for interconnecting two or more conductive layers of the carrier. Interlayer interconnection units of the invention were described hereinabove (e.g., with reference to Figures 4A-B). Formation of interlayer

interconnection units of the invention is also described herein, for example, with reference to method 400 (Figure 9).

[0070] Figure 10 schematically represents a series of steps (502-514) involved in a method 500 for making a carrier for a multilayer PCB, according to another embodiment of the present invention, wherein step 502 may involve providing a first metal layer. Step 504 may involve providing a first dielectric layer. The first metal layer may be laminated to a first side of the first dielectric layer.

[0071] Step 506 may involve forming a bridge layer. Bridge layer, which may comprise a plurality of spaced apart bridge pads, may be formed by etching a layer of copper foil laminated to a second side of the first dielectric layer. Formation of the bridge layer is described elsewhere herein, for example, with reference to method 200 (Figure 7).

[0072] Step 508 may involve providing a second dielectric layer. The second dielectric layer provided in step 508 may be laminated to the bridge layer, such that the bridge pads of bridge layer are encapsulated in dielectric material between the first and second dielectric layers. Step 510 may involve providing a second metal layer, which may be laminated to the second dielectric layer.

[0073] Step 512 may involve forming a first blind via of an interlayer interconnection unit, wherein the first blind via may be disposed between the first metal layer and a first side of a bridge pad. Step 514 may involve forming a second blind via of the interlayer interconnection unit, wherein the second blind via may be disposed between the second metal layer and a second side of the bridge pad. First and second blind vias formed on opposite sides of a bridge pad within a multilayer carrier are described hereinabove, e.g., with reference to Figures 4A-B and Figure 7.

[0074] In method 500, first and second blind vias may be plated shut in a single plating cycle, for example, as described with reference to method 200 (Figure 7). Use of a single plating cycle minimizes excessive build-up of surface copper, and therefore decreases the need for subsequent reduction of surface copper, as described hereinabove. Optionally, after forming and plating shut the first and second blind vias to form a pseudo three-layer core, one or more additional dielectric layers and metal layers may be laminated to the pseudo three-layer core (see, e.g., step 316 of method 300 (Figure 8)).

[0075] Figures 11A-E illustrate stages in forming an interlayer interconnection

unit for a multilayer PCB, according to one embodiment of the present invention. Figure 11A shows a first dielectric layer 124 which can be clad on each side with a layer of copper foil, namely a first layer of copper foil 120 and a second layer of copper foil 126'. First dielectric layer 124 may also be referred to as a metal clad first dielectric layer 124 having a first metal clad side clad with a first layer of copper foil 120, and a second metal clad side clad with a second layer of copper foil 126'. The first layer of copper foil 120 may also be referred to herein as first metal layer 120. The second layer of copper foil 126' may be etched to form a bridge layer 126 (Figures 11B-E).

[0076] Figure 11B shows a bridge pad 134, which may be formed by etching second layer of copper foil 126'. For the sake of clarity, Figures 11B-E show only one bridge pad 134 within bridge layer 126; however in practice, a much larger number of bridge pads may be formed within bridge layer 126.

[0077] Figure 11C shows the structure of Figure 11B and which may have a second dielectric layer 125 and a second metal layer 122 laminated thereto. Although Figures 11C-E show a gap 112 within bridge layer 126 adjacent to bridge pad 134, during lamination first and second dielectric layers 124, 125 may fuse around bridge pad 134 such that bridge pad 134 may be encapsulated within first and second dielectric layers 124, 125.

[0078] Figure 11D illustrates the structure of Figure 11C after etching first and second metal layers 120, 122, respectively to form capture pads 130, 132, respectively. Figure 11 D also shows a first blind via 140 and a second blind via 142. First and second blind vias 140, 142 can extend from first and second metal layers 120, 122, respectively, to first and second sides of bridge pad 134.

[0079] Figure 11E shows the structure of Figure 11D which may have solid first and second blind vias 140', 142' filled and plated shut to form interlayer interconnection unit 150 for interconnecting first and second metal layers 120, 122. An interlayer interconnection unit 150 of the invention has been described hereinabove. Briefly, interlayer interconnection unit 150 may include first capture pad 130, solid first blind via 140', bridge pad 134, solid second blind via 142', and second capture pad 132.

[0080] It should be understood, of course, that the foregoing relates to preferred embodiments of the invention and that modifications may be made without departing from the spirit and scope of the invention as set forth in the following claims.

CLAIMS

1. An interlayer interconnection unit for a printed circuit board (PCB), comprising:

an interstitial bridge pad having a first side and a second side, wherein said interstitial bridge pad is disposed between a first dielectric layer and a second dielectric layer;

a first blind via disposed on said first side of said interstitial bridge pad, wherein said first blind via extends through said first dielectric layer; and

a second blind via disposed on said second side of said interstitial bridge pad, wherein said second blind via extends through said second dielectric layer, wherein said interstitial bridge pad is adapted to electrically connect said first blind via to said second blind via.

2. The interlayer interconnection unit of claim 1, wherein said interstitial bridge pad comprises a disc-shaped conductive element.

3. The interlayer interconnection unit of claim 1, wherein:

said first blind via extends from a first conductive layer, through said first dielectric layer, and to said first side of said interstitial bridge pad, and

said second blind via extends from a second conductive layer, through said second dielectric layer, and to said second side of said interstitial bridge pad.

4. The interlayer interconnection unit of claim 1, wherein said first conductive layer and said second conductive layer each comprise copper foil.

5. The interlayer interconnection unit of claim 1, wherein:

said first blind via extends from a first capture pad to said first side of said interstitial bridge pad, and

said second blind via extends from a second capture pad to said second side of said interstitial bridge pad.

6. The interlayer interconnection unit of claim 5, wherein said first capture

pad and said second capture pad each have a diameter less than a diameter of said interstitial bridge pad.

7. The interlayer interconnection unit of claim 1, wherein said interstitial bridge pad has a diameter in the range of from about 12 to 20 mils.

8. The interlayer interconnection unit of claim 1, wherein:

said PCB comprises a bridge layer disposed between said first dielectric layer and said second dielectric layer, and

said interstitial bridge pad is located within said bridge layer, and wherein said interstitial bridge pad lacks electrical connection, within said bridge layer, to a conductive element of said bridge layer.

9. The interlayer interconnection unit of claim 1, wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via.

10. An interlayer interconnection unit for a multi-layer PCB, comprising:

a first capture pad having a first annular ring;

a first via having a first via inner end and a first via outer end, said first via outer end in contact with said first capture pad and encircled by said first annular ring;

an interstitial bridge pad having a first side and a second side, said first via inner end in contact with said first side of said interstitial bridge pad;

a second via having a second via inner end and a second via outer end, said second via inner end in contact with said second side of said interstitial bridge pad; and

a second capture pad having a second annular ring, said second via outer end in contact with said second capture pad and encircled by said second annular ring.

11. The interconnection unit of claim 10, wherein said first annular ring, said first via, said interstitial bridge pad, said second via, and said second annular ring are coaxial with each other.

12. The interconnection unit of claim 10, wherein:

said first via extends through a first dielectric layer, and

said second via extends through a second dielectric layer.

13. The interconnection unit of claim 10, wherein said interstitial bridge pad has a diameter in the range of from about 14 to 17 mils.

14. The interconnection unit of claim 10, wherein:

said multilayer PCB comprises an internal bridge layer, and

said interstitial bridge pad is a component of said bridge layer.

15. The interconnection unit of claim 10, wherein each of said first via and said second via has an aspect ratio of at least about 1:1.

16. The interconnection unit of claim 10, wherein said interconnection unit has an effective aspect ratio greater than about 2:1.

17. The interconnection unit of claim 10, wherein:

said first capture pad is located within a first conductive layer,

said second capture pad is located within a second conductive layer, and

said interconnection unit further comprises a third via extending from said first capture pad or said second capture pad to a third conductive layer.

18. A dual blind via interconnection unit for a multilayer PCB, comprising:

a pair of opposed coaxial blind vias; and

a bridge pad disposed between said pair of blind vias, wherein each of said pair of blind vias is in contact with said bridge pad, and wherein said bridge pad is adapted to electrically interconnect said pair of opposed coaxial blind vias.

19. The interconnection unit of claim 18, wherein said bridge pad has a diameter in the range of from about 12 to 20 mils.

20. The interconnection unit of claim 19, wherein each of said pair of blind vias has a diameter in the range of from about 4 to 6 mils.

21. A carrier for a multi-layer printed circuit board (PCB), said carrier comprising a pseudo three-layer core, said pseudo three-layer core including:

a first metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer; and

a second metal layer disposed on said second dielectric layer,

wherein said bridge layer comprises a plurality of spaced apart interstitial bridge pads, and

wherein at least one of said plurality of interstitial bridge pads is adapted for providing an interlayer interconnection between said first metal layer and said second metal layer.

22. The carrier of claim 21, wherein:

each of said plurality of interstitial bridge pads is connected to said first metal layer by a first blind via, and

each of said plurality of interstitial bridge pads is connected to said second metal layer by a second blind via.

23. The carrier of claim 21, wherein said bridge layer lacks an electrical connection between said plurality of interstitial bridge pads.

24. The carrier of claim 21, wherein said plurality of interstitial bridge pads are spaced apart from each other by a distance in the range of from about 0.7 to 4 mils.

25. The carrier of claim 24, wherein said plurality of interstitial bridge pads are arranged within said bridge layer at a center-to-center pitch in the range of from about 15 to 25 mils.

26. The carrier of claim 21, wherein:

said first metal layer comprises a first signal layer of said PCB, and

said second metal layer comprises a second signal layer of said PCB.

27. The carrier of claim 26, further comprising at least a third signal layer laminated to said pseudo three-layer core.

28. The carrier of claim 26, wherein said carrier comprises from 2 to 4 additional signal layers laminated to said pseudo three-layer core.

29. A pseudo three-layer core for a printed circuit board (PCB), comprising:

a plurality of interlayer interconnection units, wherein each of said plurality of interlayer interconnection units extends from a first metal layer to a second metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer; and

a second dielectric layer disposed on said bridge layer,

wherein said second metal layer is disposed on said second dielectric layer, and

wherein at least one of said plurality of interlayer interconnection units comprises:

an interstitial bridge pad located within said bridge layer;

a first blind via extending from said first metal layer to a first side of said interstitial bridge pad; and

a second blind via extending from said second metal layer to a second side of said interstitial bridge pad.

30. A multi-layer printed circuit board (PCB), comprising:

a first signal layer;

a second signal layer;

a bridge layer disposed between said first signal layer and said second signal layer; and

a plurality of interlayer interconnection units, each of said plurality of interlayer interconnection units adapted for connecting said first signal layer with said second signal layer through said bridge layer, wherein at least one said plurality of interlayer

interconnection units comprises:

a pair of opposed coaxial blind vias; and

a bridge pad disposed between, and in electrical contact with, said pair of blind vias.

31. The multi-layer PCB of claim 30, wherein:

said bridge pad includes a first side and a second side; and wherein

said pair of opposed coaxial blind vias comprise a first blind via disposed on said first side of said bridge pad, and a second blind via disposed on said second side of said bridge pad.

32. The multi-layer PCB of claim 30, further comprising at least one additional dielectric layer laminated to said first signal layer, and at least one additional signal layer laminated to said at least one additional dielectric layer.

33. A multi-layer PCB, comprising:

at least one pseudo three-layer core including:

a first metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer;

a second metal layer disposed on said second dielectric layer; and

a plurality of interlayer interconnection units for electrically interconnecting said first metal layer with said second metal layer, wherein at least one of said plurality of interlayer interconnection units comprises:

an interstitial bridge pad having a first side and a second side;

a first blind via disposed on said first side of said interstitial bridge pad; and

a second blind via disposed on said second side of said interstitial bridge pad.

34. The multilayer PCB of claim 33, wherein each of said plurality of

interlayer interconnection units is adapted for electrically interconnecting said first metal layer with said second metal layer.

35. The multilayer PCB of claim 33, wherein:

each of said first metal layer and said second metal layer comprises a signal layer, and

said multilayer PCB further comprises at least one additional signal layer laminated to said at least one pseudo three-layer core.

36. The multilayer PCB of claim 33, wherein said at least one pseudo three-layer core comprises a first pseudo three-layer core and at least a second pseudo three-layer core laminated to said first pseudo three-layer core.

37. The multilayer PCB of claim 33, wherein said multilayer PCB comprises from 1 to 4 pseudo three-layer cores and from 4 to 28 signal layers.

38. A multilayer PCB, comprising:

means for carrying a plurality of signal layers; and

means for interconnecting at least two of said plurality of signal layers,

wherein said carrying means comprises a pseudo three-layer core,

wherein said pseudo three-layer core includes an internal bridge layer that comprises a plurality of interstitial bridge pads, and

wherein said interconnecting means comprises a pair of opposed blind vias disposed on either side of each of said plurality of interstitial bridge pads.

39. The multilayer PCB of claim 38, wherein:

said bridge layer comprises an internal pseudo metal layer disposed between a first dielectric layer and a second dielectric layer, and

wherein said interconnecting means is adapted for interconnecting said plurality of signal layers.

40. A method for forming a multilayer printed circuit board (PCB), comprising:

a) providing a metal clad first dielectric layer having a first metal clad side and a second metal clad side;

b) forming a bridge layer from said second metal clad side, wherein said bridge layer comprises a plurality of bridge pads, and wherein said first metal clad side comprises a first metal layer;

c) providing a second dielectric layer on said bridge layer, wherein said second dielectric layer has a second metal layer disposed thereon;

d) forming a first blind via through said first dielectric layer, wherein said first blind via extends from said first metal layer to a first side of at least one of said plurality of bridge pads; and

e) forming a second blind via through said second dielectric layer, wherein said second blind via extends from said second metal layer to a second side of said at least one of said plurality of bridge pads.

41. The method of claim 40, wherein said step b) comprises etching said second metal clad side of said first dielectric layer to form said at least one of said plurality of bridge pads.

42. The method of claim 40, wherein:

said second metal clad side comprises copper foil, and

wherein said at least one of said plurality of bridge pads comprises copper.

43. The method of claim 40, wherein each of said plurality of bridge pads has a diameter in the range of from about 12 to 20 mils.

44. The method of claim 40, wherein said bridge layer lacks electrical connectivity between said plurality of bridge pads.

45. The method of claim 40, wherein said steps c) and d) respectively comprise forming said first blind via and said second blind via by a process selected from the group consisting of laser drilling, plasma drilling, and photo-defining.

46. The method of claim 40, further comprising:

e) plating shut said first blind via and said second blind via.

47. The method of claim 40, wherein said method involves only a single plating cycle.

48. The method of claim 46, wherein after said step e), said first metal layer and said second metal layer each have a thickness in the range of from about 0.8 to 1.4 mils.

49. The method of claim 46, wherein after said step e) said first metal layer and said second metal layer each have a thickness in the range of from about 0.9 to 1.1 mils.

50. The method of claim 40, wherein said first blind via and said second blind via each comprise a μvia having a diameter in the range of from about 4 to 5 mils.

51. A method for forming a multilayer printed circuited board (PCB), comprising:

a) forming a pseudo three-layer core, said pseudo three-layer core including:

a first metal layer;

a first dielectric layer disposed on said first metal layer,

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer; and

a second metal layer disposed on said second dielectric layer, wherein said bridge layer comprises a plurality of spaced apart interstitial bridge pads; and

b) forming a plurality of interlayer interconnection units for interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes:

a first blind via disposed on a first side of one of said plurality of interstitial bridge pads, wherein said first blind via extends from said first metal layer

through said first dielectric layer; and

a second blind via disposed on a second side of one of said plurality of interstitial bridge pads, wherein said second blind via extends from said second metal layer through said second dielectric layer.

52. The method of claim 51, wherein:

said step b) comprises plating shut said first blind via and said second blind via, and

said method includes only a single plating cycle.

53. The method of claim 51, wherein each of said first blind via and said second blind via has an aspect ratio of at least about 1:1.

54. The method of claim 53, wherein each of said interlayer interconnection units has an effective aspect ratio of at least about 2:1.

55. A method for forming a multilayer printed circuit board (PCB), comprising:

a) a step for forming a pseudo three-layer core, wherein said pseudo three-layer core includes:

a first metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer; and

a second metal layer disposed on said second dielectric layer; and

b) a step for forming a plurality of interlayer interconnection units for electrically interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes:

a pair of opposed coaxial blind vias, and

a bridge pad disposed between, and in electrical contact with, said pair of blind vias, wherein said bridge layer comprises a plurality of said bridge pads.

56. A method for forming a pseudo three-layer core for a PCB, comprising:

a) providing a first metal layer;

b) providing a first dielectric layer on said first metal layer;

c) forming a bridge layer on said first dielectric layer, said bridge layer comprising a plurality of bridge pads;

d) providing a second dielectric layer on said bridge layer;

e) providing a second metal layer on said second dielectric layer;

f) forming a first blind via on a first side of each of said plurality of bridge pads, wherein said first blind via extends from said first metal layer through said first dielectric layer; and

g) forming a second blind via on a second side of each of said plurality of bridge pads, wherein said second blind via extends from said second metal layer through said second dielectric layer.

57. The method of claim 56, wherein:

said first dielectric layer comprises a first side and a second side, said first side having said first metal layer disposed thereon, and said second side having a layer of copper foil disposed thereon, and

said step c) comprises etching said layer of copper foil.

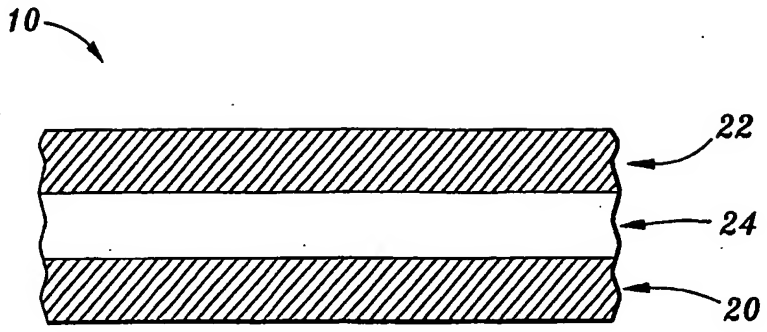


FIG. 1A
(PRIOR ART)

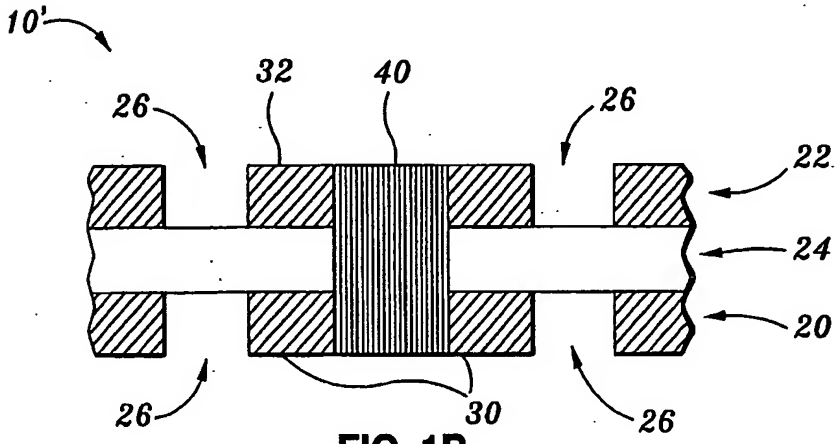


FIG. 1B
(PRIOR ART)

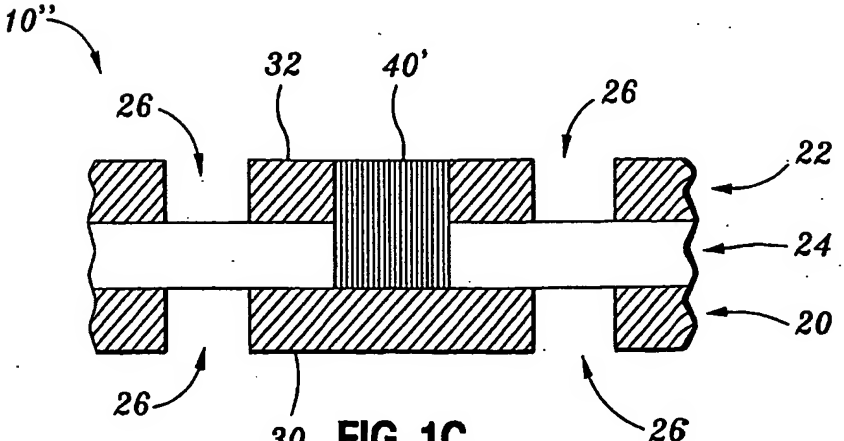


FIG. 1C
(PRIOR ART)

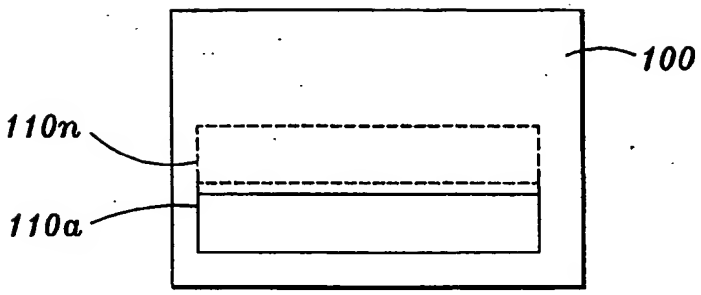
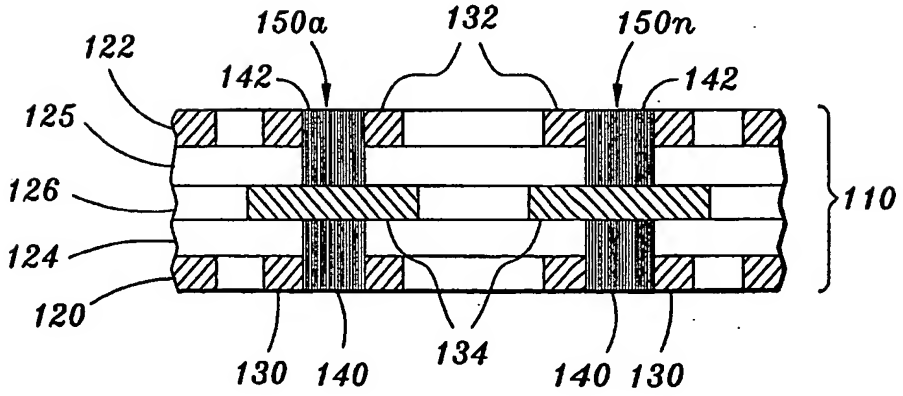

100
110n
110a

FIG. 2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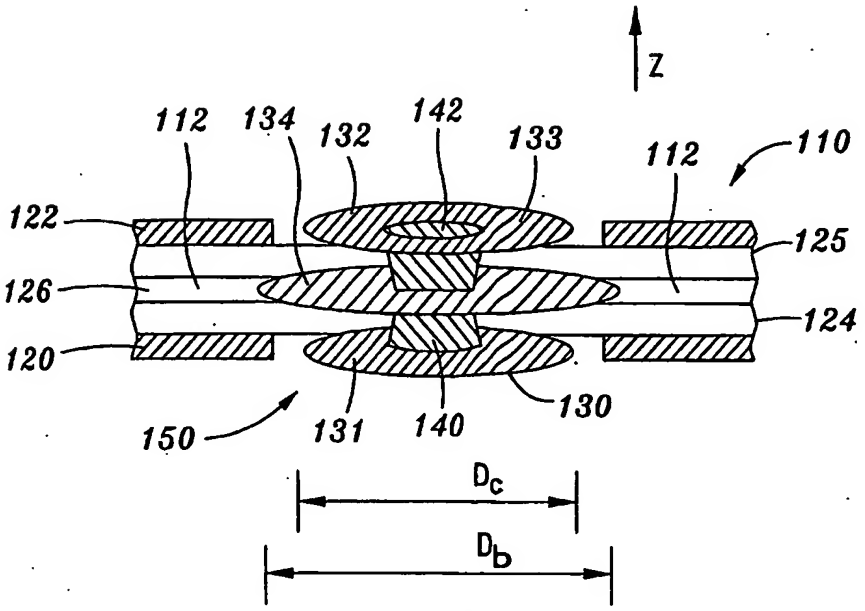
140
130

FIG. 3


Z
112
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124
120
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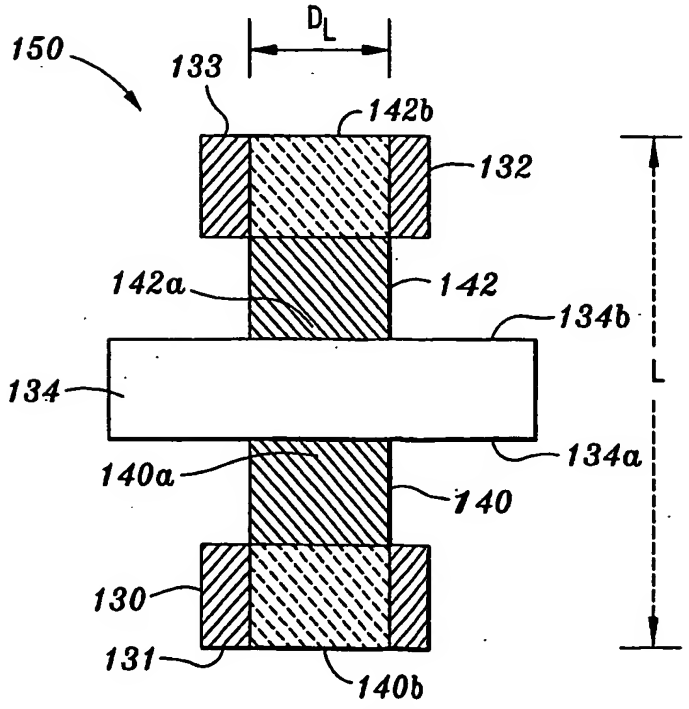
150
131
140
D_c
D_b

FIG. 4A


D_L
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142a
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L
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131
140b

FIG. 4B

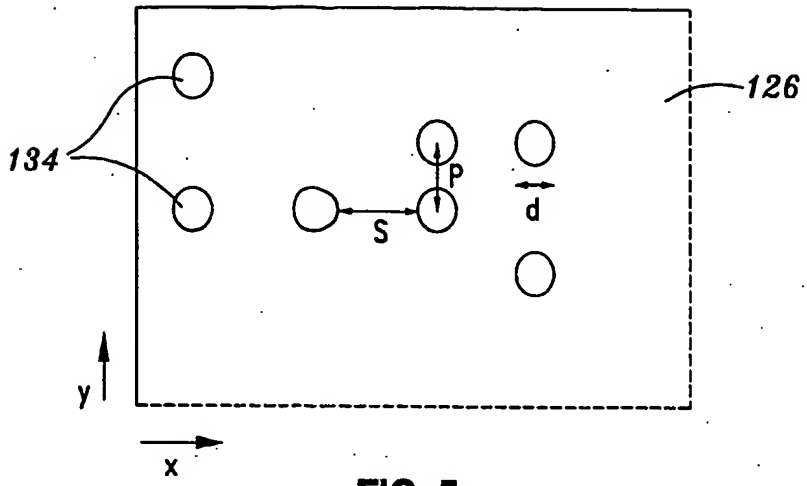


FIG. 5

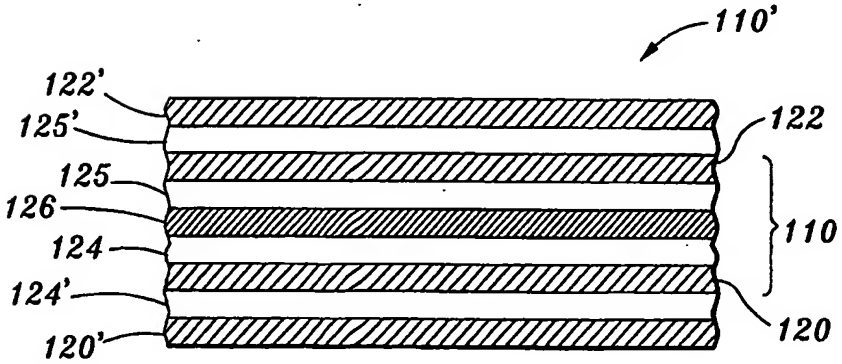


FIG. 6

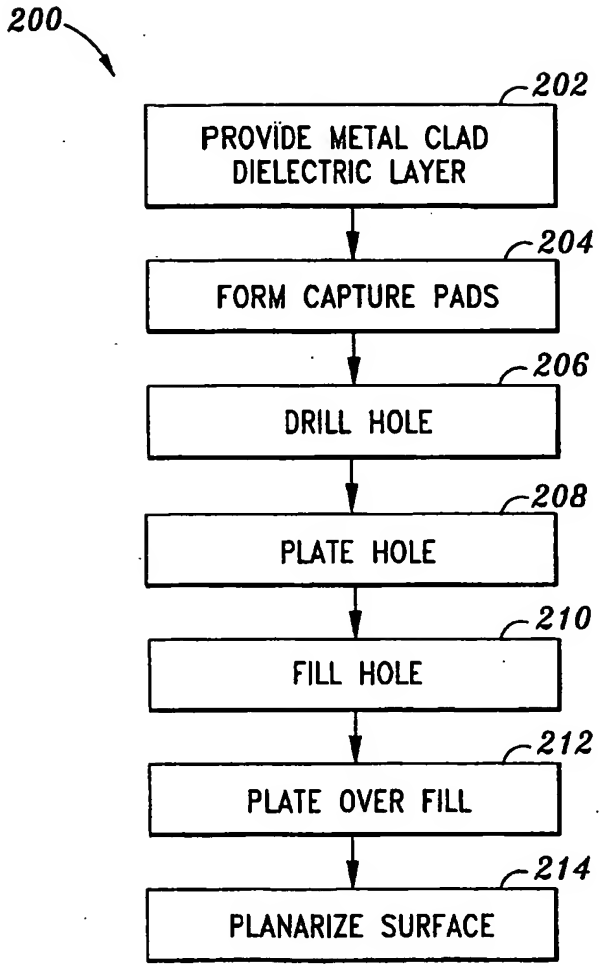


FIG. 7

(PRIOR ART)

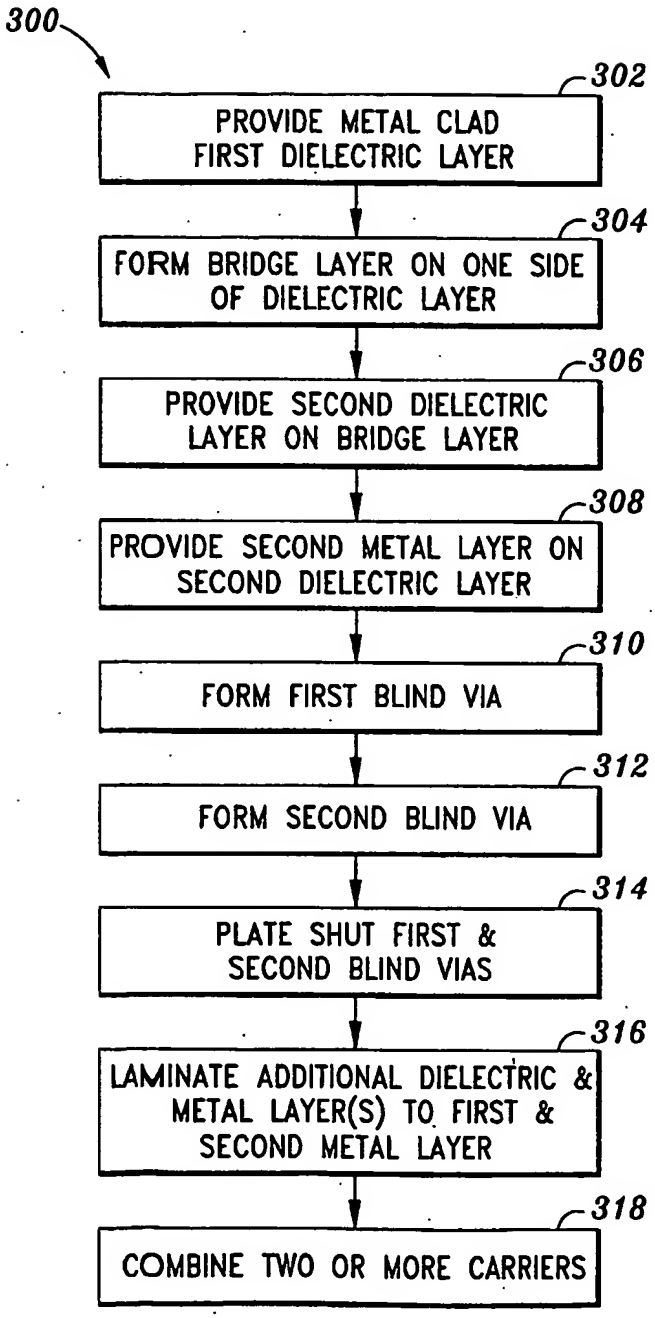

300
302
PROVIDE METAL CLAD FIRST DIELECTRIC LAYER
304
FORM BRIDGE LAYER ON ONE SIDE OF DIELECTRIC LAYER
306
PROVIDE SECOND DIELECTRIC LAYER ON BRIDGE LAYER
308
PROVIDE SECOND METAL LAYER ON SECOND DIELECTRIC LAYER
310
FORM FIRST BLIND VIA
312
FORM SECOND BLIND VIA
314
PLATE SHUT FIRST & SECOND BLIND VIAS
316
LAMINATE ADDITIONAL DIELECTRIC & METAL LAYER(S) TO FIRST & SECOND METAL LAYER
318
COMBINE TWO OR MORE CARRIERS

FIG. 8

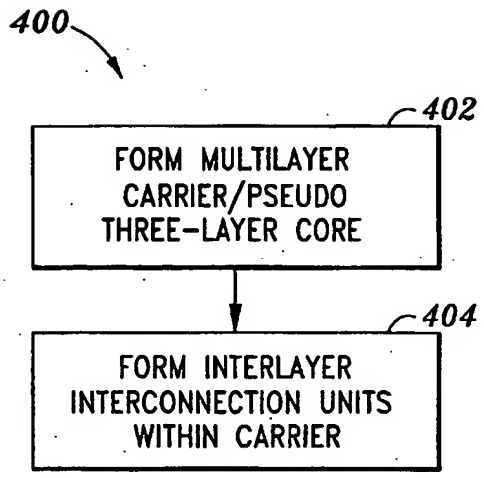
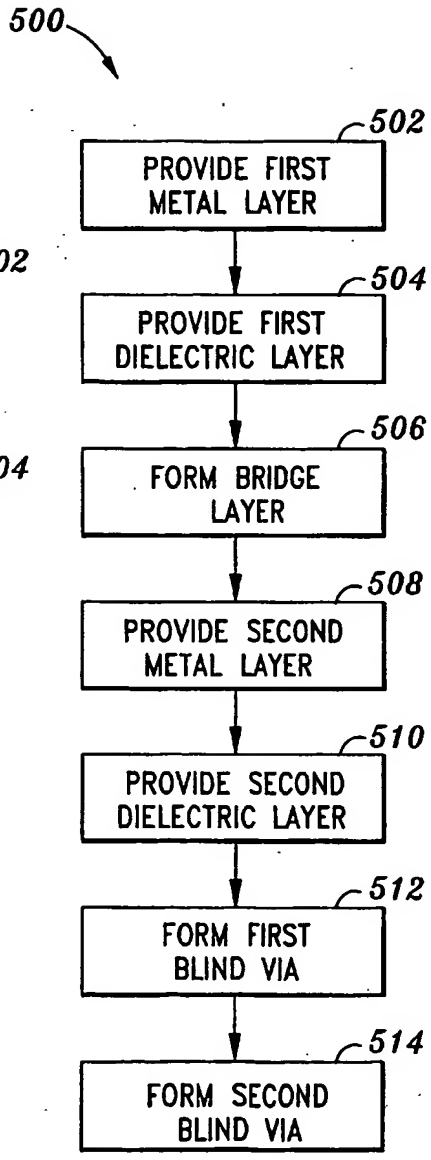

400
402
FORM MULTILAYER CARRIER/PSEUDO THREE-LAYER CORE
404
FORM INTERLAYER INTERCONNECTION UNITS WITHIN CARRIER

FIG. 9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PROVIDE FIRST DIELECTRIC LAYER
506
FORM BRIDGE LAYER
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PROVIDE SECOND DIELECTRIC LAYER
512
FORM FIRST BLIND VIA
514
FORM SECOND BLIND VIA

FIG. 10

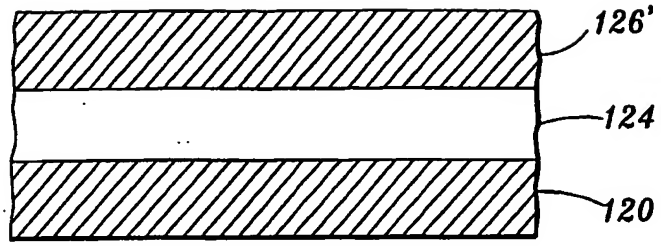

FIG. 11A

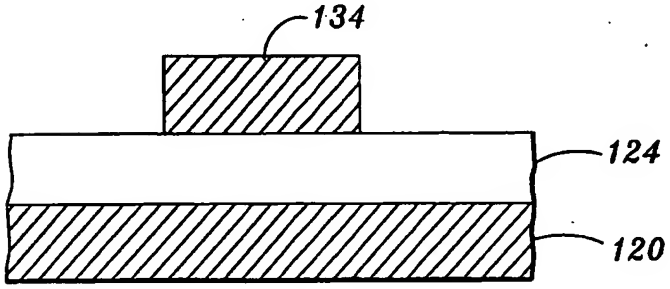

FIG. 11B

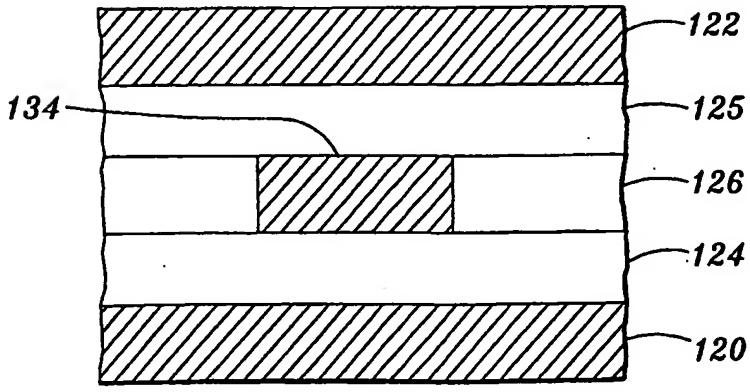

FIG. 11C

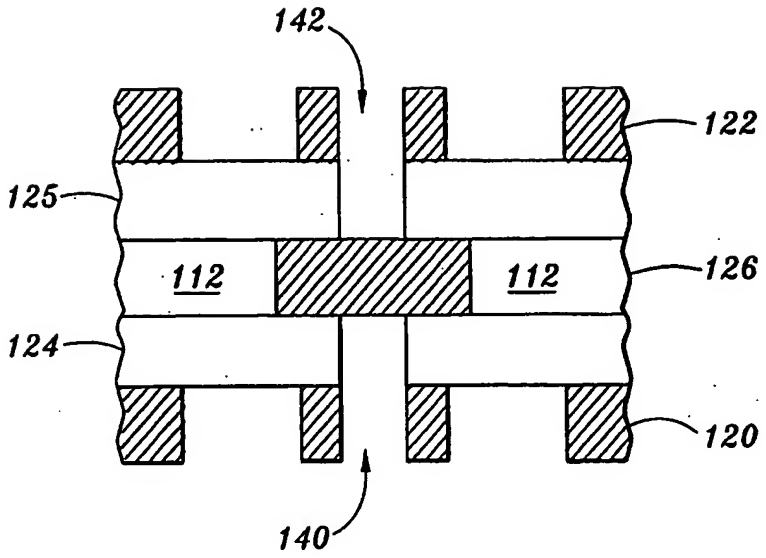

FIG. 11D

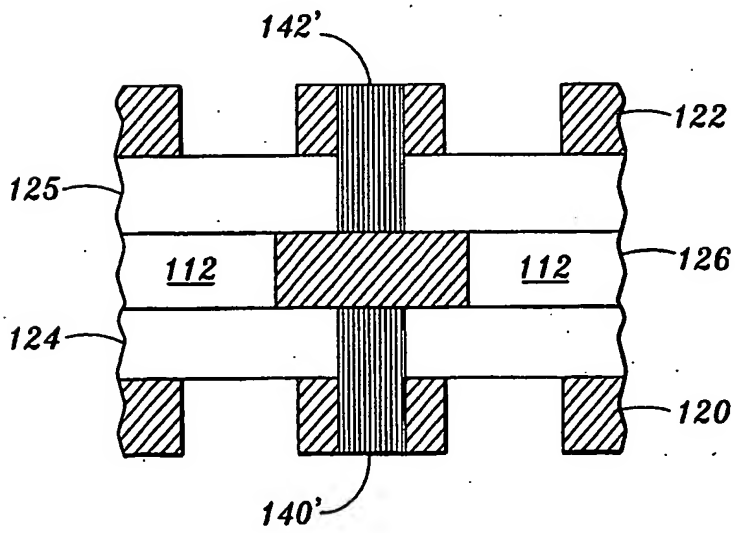

FIG. 11E

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/033012

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05K1/11 H05K3/42 H05K3/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05K H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 2003, no. 05, 12 May 2003 (2003-05-12) & JP 2003 031952 A (MEIKO:KK), 31 January 2003 (2003-01-31) abstract	1-57
P,X	-& EP 1 406 477 A (MEIKO ELECTRONICS CO., LTD) 7 April 2004 (2004-04-07) paragraphs '0023! - '0040!; figures 8-14	1-57
X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 14, 22 December 1999 (1999-12-22) & JP 11 261236 A (ELNA CO LTD), 24 September 1999 (1999-09-24) abstract	1-57

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 February 2005	25/02/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax (+31–70) 340–3016	Batev, P

1

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/033012

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 471 631 A (LEO J. QUINTANA) 7 October 1969 (1969-10-07) the whole document	1-57
X	US 5 347 712 A (YASUDA ET AL) 20 September 1994 (1994-09-20) column 13, line 61 - column 14, line 15; figures 21,22	1-57
X	US 6 548 767 B1 (LEE KYU-WON ET AL) 15 April 2003 (2003-04-15) the whole document	1-57
X	US 5 846 097 A (MARIAN, JR. ET AL) 8 December 1998 (1998-12-08) column 7, line 50 - column 8, line 15; figure 5	1,21,29, 33,40, 51,56

1

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/033012

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JP 2003031952	A	31-01-2003	EP	1406477	A1	07-04-2004
			WO	03009661	A1	30-01-2003
			US	2004136152	A1	15-07-2004
EP 1406477	A	07-04-2004	JP	2003031952	A	31-01-2003
			EP	1406477	A1	07-04-2004
			US	2004136152	A1	15-07-2004
			WO	03009661	A1	30-01-2003
JP 11261236	A	24-09-1999	NONE			
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